

1. DESCRIPTION

MT5702LP is a System on Chip (SoC) for magnetic induction based wireless power receiver.

It is capable of wireless charging for up to 10W(10V/1A) and can be configured as a wireless charging transmitter to charge other receivers. It is fully compliant with WPC Qi Specification (Version 2.1) of BPP (Baseline Power Profile) and also supports various proprietary fast charging protocols used by major smartphone OEM's.

MT5702LP has a very high overall AC to DC conversion efficiency (up to 95%), thanks to the optimized and adaptive full synchronous rectifier control, very small $R_{DS(on)}$ of power MOSFET, and extremely low bias current are achieved.

The AC input can be converted to fully programmable DC output voltage due to the magnetic induction charging technology.

Designed with ARM Cortex M0 processor, integrated with optimized and adaptive full synchronous rectifier control and special LDO, the chip achieves high efficiency, ultra-low bias current and very small power MOSFET $R_{DS(on)}$.

MT5702LP is embedded with various protection features, such as FOD, over-voltage, over-current and over-temperature protection which guarantee the system reliability.

2. APPLICATIONS

- Wearable devices with high integration and small form factor
- Rx function for power banks where they can be wirelessly charged
- Other wireless power applications

3. FEATURES

- Power delivery: up to 10W(10V/1A)
- Fully programmable output voltage from 3V to 12V in 25mV per step or 3V to 6V in 12mV per step and supporting current limit
- Embedded with ARM Cortex M0 processor with 6kB SRAM and 512bytes OTP, 16kB ROM
- 85kHz~500kHz wide wireless charging frequency
- Supports 1.8V I/O and 1.2V I/O
- Embedded with various protection features:
 - over-voltage protection (OVP)
 - over-current protection (OCP)
 - short-circuit protection (SCP)
 - over-temperature protection (OTP)
 - foreign object detection (FOD)
- Innovative output LDO with output clamping and fast response to line and load transient
- Integrated flexible sink function with internal and external module
- Qi 2.1 compliant and proprietary communication protocols support with hardware ASK modulation and FSK demodulation
- Independent I²C slave interface with additional GPIO's
- Halogen free and RoHS compliant
- Available in QFN16L (2.310mm x 2.390mm) package

4. TYPICAL APPLICATION CIRCUIT

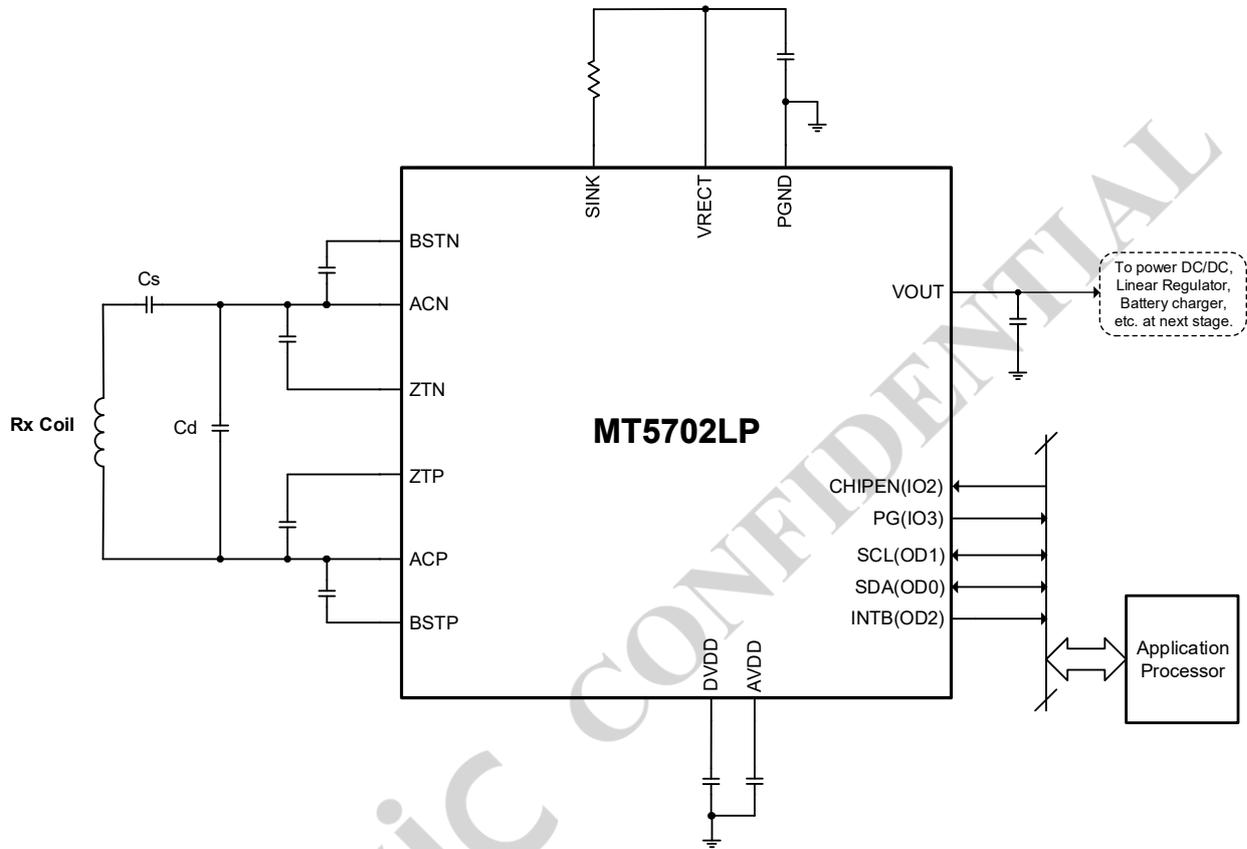


Figure 1 Typical Application Circuit

Content

1.	DESCRIPTION.....	1
2.	APPLICATIONS	1
3.	FEATURES	1
4.	TYPICAL APPLICATION CIRCUIT	2
5.	PIN CONFIGURATIONS AND FUNCTIONS	4
5.1.	Pin Configuration	4
5.2.	Pin Functions	5
6.	SPECIFICATIONS	6
6.1.	Absolute Maximum Ratings	6
6.2.	ESD Ratings	6
6.3.	Recommended Operating Conditions	7
6.4.	Package Thermal Information	7
7.	DETAILED DESCRIPTIONS	7
7.1.	Functional Block Diagram	10
7.2.	Theory of Operation.....	10
7.3.	Rectifier Bridge	11
7.4.	LDO Regulator.....	11
7.5.	ADC Converter	11
7.6.	Digital Unit	11
7.7.	I ² C.....	12
7.7.1.	I ² C Interface.....	12
7.7.2.	I ² C Timing Characteristics	12
7.7.3.	ID and Address.....	13
7.7.4.	I ² C Write/Read Protocol	13
7.8.	Foreign Object Detection (FOD).....	13
7.9.	Other Blocks	13
8.	DETAILED PACKAGING INFORMATION.....	14
9.	REVISION HISTORY	15
	IMPORTANT NOTICE	16

5. PIN CONFIGURATIONS AND FUNCTIONS

5.1. Pin Configuration

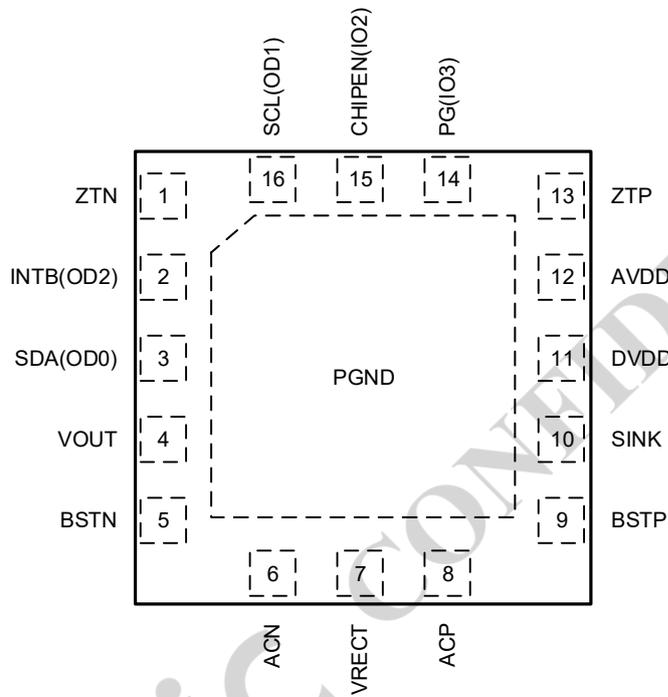


Figure 2 Top View

5.2. Pin Functions

Table 1 Pin Functions

Name	Location	Description
ZTN	1	ASK modulation FET at ACN. Recommend to connect a 22nF capacitor between this pin and ACN.
INTB(OD2)	2	GPOD & Interrupt. This is the interrupt from wireless power to AP.
SDA(OD0)	3	I2C slave SDA.
VOUT	4	Output of power LDO. Recommend to connect one 10 μ F capacitors between this pin and GND.
BSTN	5	Boost capacitor for internal driver for bridge rectifier at ACN. Recommend to connect a 47nF capacitor between this pin and ACN.
ACN	6	AC negative input, connect to the other end of the resonant tank.
VRECT	7	Output of synchronous rectifier. Recommend to connect two 10 μ F capacitors between this pin and GND.
ACP	8	AC positive input, connect to one end of the resonant tank.
BSTP	9	Boost capacitor for internal driver for bridge rectifier at ACP. Recommend to connect a 47nF capacitor between this pin and ACP.
SINK	10	Providing sinking current. Recommend to connect a 200 Ω resistor between this pin and VRECT.
DVDD	11	Internal 1.5V power supply. Recommend to connect a 1 μ F capacitor between this pin and GND.
AVDD	12	5.0V LDO's output, local power supply for internal analog circuit.
ZTP	13	ASK modulation FET at ACP. Recommend to connect a 22nF capacitor between this pin and ACP.
PG(IO3)	14	Power good pin to AP, default open drain, After RX send Qi 71 package, pull the Pin PG(IO3) low.
CHIPEN(IO2)	15	After detect the Pin CHIPEN(IO2) high in RX mode, send EPT 02 0B three times to TX, then not communication to TX.
SCL(OD1)	16	I ² C slave SCL.
PGND	Bottom plane	Power ground.

6. SPECIFICATIONS

6.1. Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings

Pin Name	Rating
ACN, ACP, ZTP, ZTN	-0.3V to 20V
BSTP with respect to ACP	-0.3V to 5.5V
BSTN with respect to ACN	-0.3V to 5.5V
VRECT	-0.3V to 20V
VOUT	-0.3V to 20V
SINK	-0.3V to 20V
AVDD	-0.3V to 5.5V
DVDD	-0.3V to 1.65V
GPOD0(SDA), GPOD1 (SCL), GPOD2(INTB), CHIPEN(IO2), PG(IO3)	-0.3V to 5.5V
Storage Temperature (T _{STG})	-55°C to 150°C
Maximum Soldering Temperature (Reflow, Pb-Free)	260°C

Note:

- Stresses greater than those listed as Absolute Maximum Ratings could cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods might affect reliability.
- All voltages are referred to ground unless otherwise stated.

6.2. ESD Ratings

Table 3 ESD Ratings

Test model	Pins	Rating
HBM	All pins	2000V
CDM	All pins	1000V
LU	All pins	250mA

6.3. Recommended Operating Conditions

Table 4 Recommended Operating Conditions

Parameter	Rating
Operating Temperature (Environment)	-40°C ~ 85°C
Operating Current (I _{OUT})	0A ~ 1.0A
Operating Voltage (V _{OUT})	3V ~ 12V

6.4. Package Thermal Information

Table 5 Package Thermal Information

Parameter	Value
Junction to ambient (R _{θJA})	45°C/W

6.5. Electrical Characteristics

Test conditions: V_{RECT}=5V, T_A=25°C, unless otherwise stated.

Table 6 Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Startup (VDD Pin)						
V _{UVLO}	Under voltage lockout	V _{RECT} rising from 0V		2.6		V
V _{UVLO_HYS}	Under voltage lockout hysteresis	V _{RECT} falling		150		mV
Supply Current						
I _Q	Quiescent current in normal operation mode	V _{RECT} = 6V			5	mA
Over-voltage Protection						
VOVP1	OVP threshold for V _{RECT} , Sink	programmable, 10V-25.5V		14		V
VOVP2	OVP threshold for V _{RECT} , Short lowside MOS	programmable, 11V-26.5V		16		V
V _{LSB_OVP} ^①	Least significant bit at OVP			500		mV

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Power LDO						
VOUT_5V	Output voltage when programming to 5V	V _{RECT} =5.5V, I _{OUT} =10mA	4.95	5	5.05	V
VOUT_9V	Output voltage when programming to 9V	V _{RECT} =10V, I _{OUT} =10mA	8.95	9	9.05	V
VOUT_12V	Output voltage when programming to 12V	V _{RECT} =13V, I _{OUT} =10mA	11.95	12	12.05	V
V _{LSB_VOUT}	Least significant bit when programming output voltage	V _{OUT} range: 3V~12V		25		mV
		V _{OUT} range: 3V~6V		12		mV
V _{PR_VOUT}	Programming range of output voltage			3~12		V
R _{DS(ON)}	R _{DS(ON)} of power MOSFETs in the power LDO	T _A =25°C		58		mΩ
Rectifier Bridge						
R _{BRG}	R _{DS(ON)} of power MOSFETs in the rectifier bridge	T _A =25°C		58		mΩ
ADC						
N	Resolution			12		Bit
f _{SAMPLE}	Sampling rate			67		kS/s
Channel	Number of channels			8		
AccVRECT	Sampling accuracy for VRECT	V _{RECT} =9V	-1		1	%
AccVOUT	Sampling accuracy for VOUT	V _{OUT} =9V	-1		1	%
AccIOUT	Sampling accuracy for IOUT	I _{OUT} ≤500mA	-5		5	mA
		I _{OUT} >500mA	-1		1	%
Miscellaneous						
AVDD	AVDD output voltage	V _{RECT} =6V, AVDD load=10mA	4.7	5	5.3	V

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DVDD	DVDD output voltage	$V_{RECT}=5V$, DVDD load=10mA	1.4	1.5	1.6	V
Digital I/O Pins						
V_{IH}	Input voltage threshold for logic High	1.8V Level	1.1			V
		1.2V Level	0.7			
V_{IL}	Input voltage threshold for logic Low	1.8V Level			0.7	V
		1.2V Level			0.46	
$V_{OH}^{\textcircled{2}}$	High level output voltage	1.8V Level, $I_{SINK}=2mA$	1.3			V
		1.2V Level, $I_{SINK}=0.15mA$	0.9			V
V_{OL}	Low level output voltage	$I_{SOURCE}=2mA$			200	mV
I_{GPIO_LKG}	Leakage current of CHIPEN(IO2), PG(IO3)	$V_{GPIOX}=1.8V$			0.5	μA
I_{GPOD_LKG}	Leakage current of GPOD0(SDA), GPOD1 (SCL), GPOD2(INTB),	$V_{GPODX}=1.8V$			0.5	μA
V_{AIR}	Analog input range			0~1.8		V

Note:

- ① Guaranteed by design.
- ② Only for push/pull type I/O.

7. DETAILED DESCRIPTIONS

7.1. Functional Block Diagram

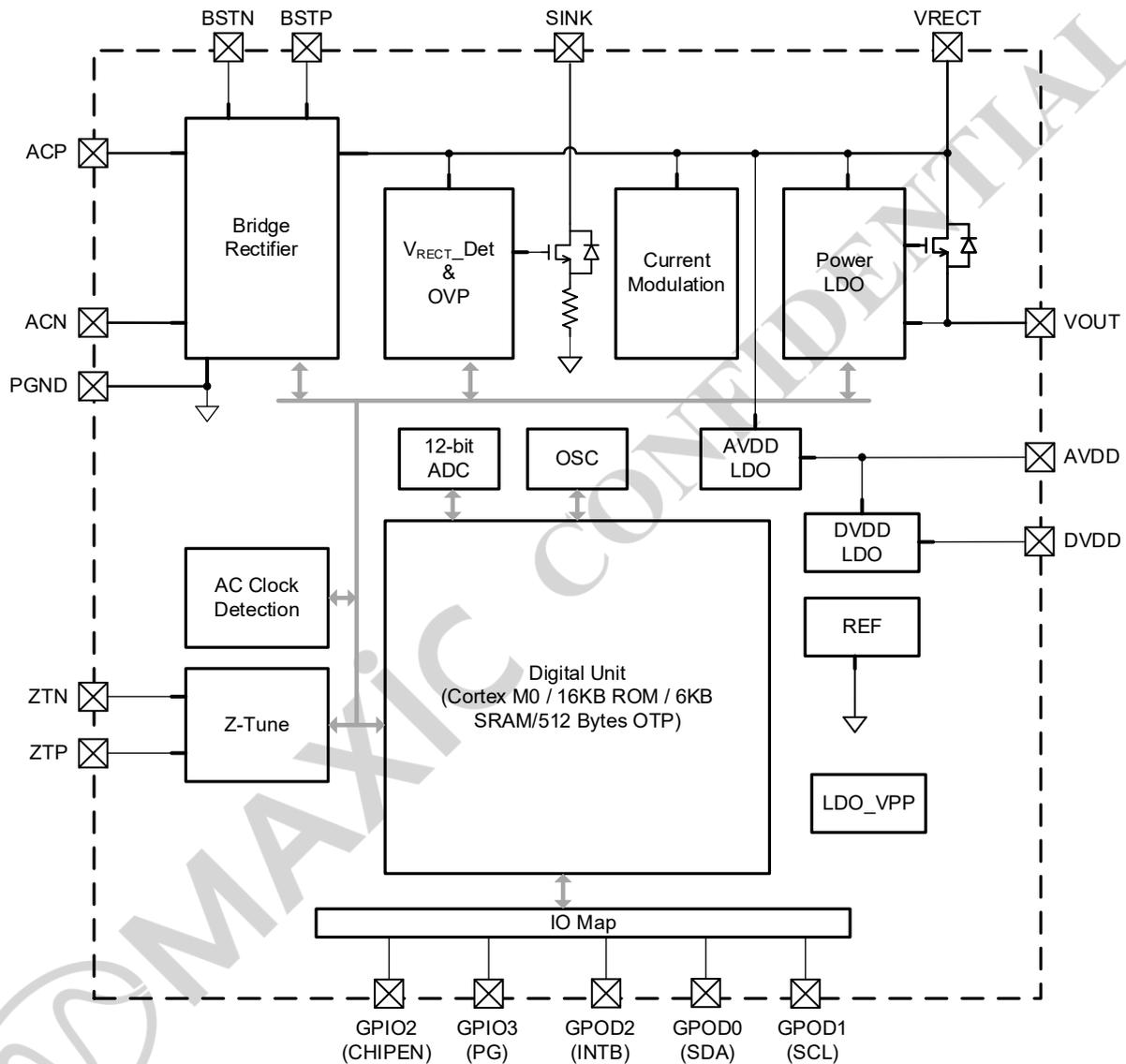


Figure 3 Functional Block Diagram

7.2. Theory of Operation

MT5702LP is a System on Chip (SoC) for wireless power receiver. It only needs several passive components, like power receiving coil, resonant tank capacitor, decoupling capacitor and pull-up/down resistors to build a complete wireless power receiver system. When coupled with a wireless power transmitter, this system can provide all the functions for wireless power transfer, including power receiving and rectification, output regulation, communication for power control and data exchange, and abnormal condition (FOD, over voltage, current, temperature, etc.) protection.

MT5702LP is by default programmed to be fully compliant with WPC Qi Specification (Version 2.1) with support of BPP (Baseline Power Profile). It can also be programmed to be compliant with major smart phone vendors' proprietary fast wireless charging protocols.

MT5702LP is composed of several major functional blocks which together achieve the wireless power receiving function.

7.3. Rectifier Bridge

MT5702LP uses an integrated high efficiency full-wave synchronous rectifier bridge to convert AC signal from the resonant tank to DC signal on the VRECT pin. During startup, the rectifier bridge operates as a passive diode bridge, and goes into bridge rectifier mode as VRECT pin voltage exceeds V_{UVLO} . If VRECT pin voltage is too high, over-voltage protection is triggered.

Moreover, MT5702LP can be configured to full-wave mode and half-wave mode by controlling the RTM pin. Once configured to half-wave mode, low inductance coils can be used, and approximately double gain can be achieved.

7.4. LDO Regulator

MT5702LP integrates three LDOs: Power LDO, AVDD LDO and DVDD LDO.

- Power LDO creates power path from VRECT to VOUT. This block functions as a load switch (connecting and disconnecting the external load), output voltage and current regulation, and output clamping when fast load/line transient happens.
- AVDD LDO and DVDD LDO provide necessary regulated analog and digital power supplies separately from rectifier output for the operation of the chip.

7.5. ADC Converter

This block is one of the key blocks that converts various measured analog variables (voltage, current, temperature, external analog inputs, etc.) to digital domain such that the embedded microcontroller can use the information for follow-up actions.

7.6. Digital Unit

This block contains all the digital circuits, including embedded microcontroller, volatile and non-volatile memories, I²C interfaces, peripherals, Direct Memory Access (DMA), internal buses, and other digital functional blocks. Digital unit is the brain of chip which dynamically configures the chip for different functions in different states, communicates with the external host, and performs necessary data processing for proper operation (such as FOD calculation, target V_{RECT} and V_{OUT} calculation, etc.).

7.7. I²C

7.7.1. I²C Interface

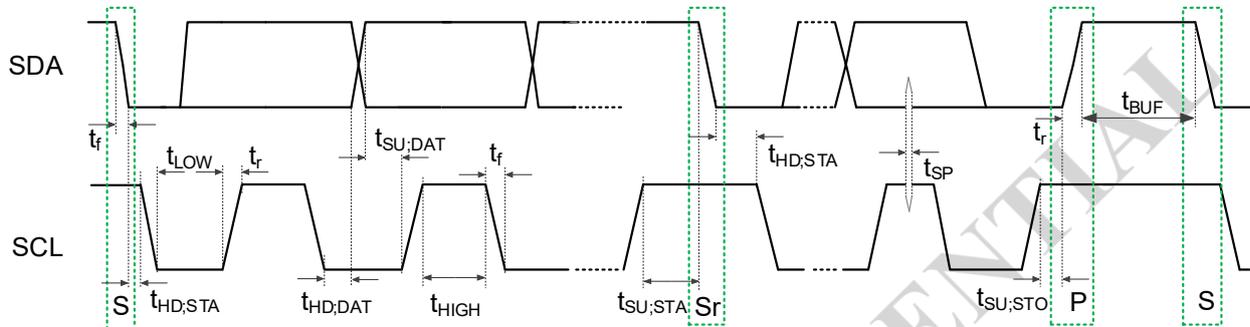


Figure 4 I²C Interface

7.7.2. I²C Timing Characteristics

All specifications are at $V_{IO} = 1.8V$, $T_{OPE} = 25^{\circ}C$, unless otherwise noted.

Table 7 I²C Timing Characteristics

Symbol	Parameter (*)	Min.	Max.	Unit
f_{SCL}	SCL clock frequency	1	400	kHz
t_{BUF}	Bus free time between STOP and the following START condition	1.3		μs
$t_{HD;STA}$	Hold time (repeated) in START condition. After this period, the first clock pulse is generated	0.6		μs
t_{LOW}	Low period of the SCL clock	1.3		μs
t_{HIGH}	High period of the SCL clock	0.6		μs
$t_{SU;STA}$	Set-up time for a repeated START condition	0.6		μs
$t_{SU;STO}$	Set-up time for STOP condition	0.6		μs
t_r	Rise time of both SDA and SCL signals		300	ns
t_f	Fall time of both SDA and SCL signals		300	ns
$t_{HD;DAT}$	Data hold time	50		ns
$t_{SU;DAT}$	Data setup time	100		ns
t_{SP}	Pulse width of spikes which must be suppressed by the input filter	0	50	ns

Note:

(*) Specified by design and characterization; not production tested.

7.7.3. ID and Address

I²C ID has 7 bits and identifies which I²C is valid. The last bit is the read/write bit and is appended by the host. The default I²C slave address is 0101011X, where X indicates read and write privileges, can be configured as:

- 0: write, equals to 0x56 in HEX.
- 1: read, equals to 0x57 in HEX.

7.7.4. I²C Write/Read Protocol

Write: 0x56 + ADDR[15:8] + ADDR[7:0] + DATA0 + DATAn

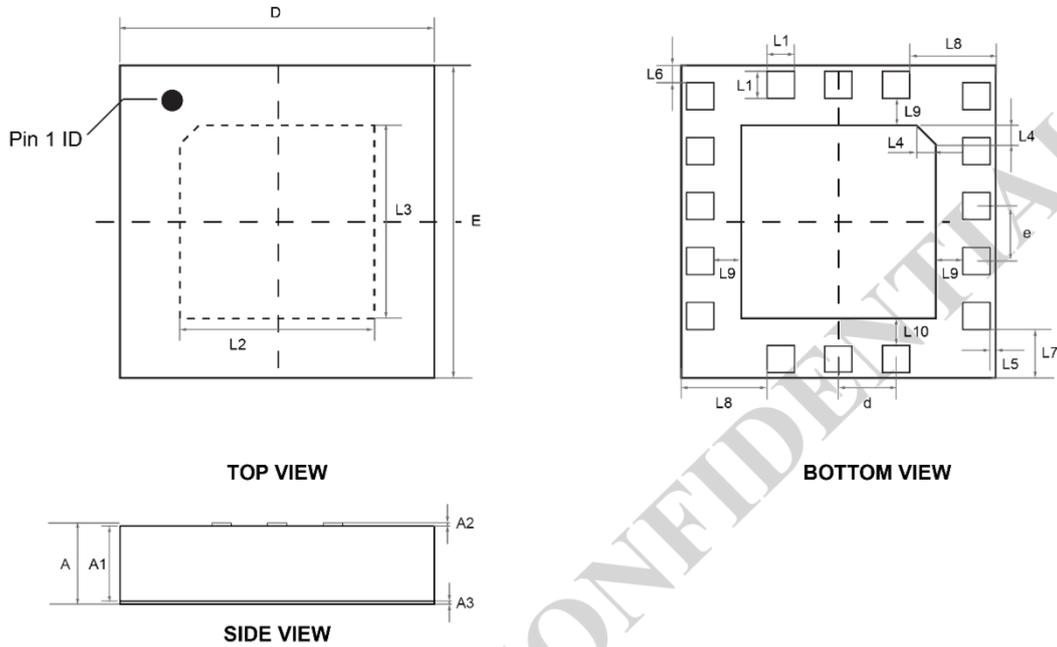
Read: 0x56 + ADDR[15:8] + ADDR[7:0] + 0x57 + DATA0 + DATAn

7.8. Foreign Object Detection (FOD)

During power transfer phase, the receiver periodically communicates with the transmitter about the amount of power received, the transmitter compares this power with the power transmitted at the same time. By comparing the power difference, the chip can confirm whether foreign object exists.

7.9. Other Blocks

- Z-Tune and CLK Detector. These blocks are for bi-directional communication for power control and data exchange.
- OSC and REF. These blocks provide the timing reference and voltage reference for the whole chip.

8. DETAILED PACKAGING INFORMATION


	A	A1	A2		A3	D	E	L1	L2	L3	L4	L5	L6	L7	L8	L9	L10	d	e	UNIT	
			CU	SN																	
MAX	0.800	0.711	0.025			2.335	2.415	0.210	1.360	1.420											
NOM	0.750	0.680	0.020	0.007~0.020	0.005~0.045	2.310	2.390	0.200	1.350	1.410	0.155	0.030	0.090	0.300	0.605	0.250	0.270	0.450	0.450	mm	
MIN	0.700	0.649	0.015			2.285	2.365	0.190	1.340	1.400											

9. REVISION HISTORY

Table 8 Revision History

Revision	Date	Description
0.01	2025-09-24	Preliminary version.
0.02	2025-09-29	Update pin configuration.
0.03	2025-11-13	Modify detailed description.
1.00	2025-11-27	Update detailed description.

IMPORTANT NOTICE

- Maxic Technology Incorporated (Maxic) reserves the right to make correction, modifications, enhancements, improvements and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to Maxic's terms and conditions of sale supplied at the time of order acknowledgement.
- Reproduction, copying, transferring, reprinting this paper without Maxic's written permission is prohibited.
- Maxic assumes no liability for applications assistance or the design of customers' products. Maxic warrants the performance of its products to the specifications applicable at the time of sale. Customers are responsible for their products and applications using Maxic components. To minimize the risks associated with customers' products and applications, customers should provide adequate design and operating safeguards.