CWT2043® Datasheet

Qi Compliant 15W
Wireless Power Transmitter SoC

General Description

CWT2043 can deliver up to 15W as a highly integrated single-chip wireless medium power transmitter IC. It can be configured to receive its input power from USB or AC adapter. Our chip integrates a power amp driver, a precise clock generator for PA frequency control, and communication controllers which use Amplitude Shift Keying (ASK) and Frequency Shift Keying (FSK). CWT2043 can support multi-coil transmitter with CWP1500 companion PA chip and it also can support precise fixed frequency PA operation with external crystal. This chip includes a 32-bit ARM Cortex M0 processor and a 1M-bit Flash memory in order to offer high level of programmability according to its applications. Communication and control units (CCU) can accommodate WPC protocol including fault condition handling associated with power transfer. The CCU supports the foreign object detection (FOD) extension. Also, the chip includes over-temperature and voltage protection.

Features Overview

- **WPC-1.2.4 compliant for MP-A11/MP-A13 medium power specification**
- **High-efficiency power transfer system supporting baseline power profile (<5W) and extended power profile (<15W)**
- **Input operating voltage of 4.5V to 20V, supporting USB**
- **Integrated pre-amplify drivers for external power amp**
- **Support multi-coil transmitter with CWP1500 companion PA chip**
- **Support up to 17 GPIO ports for multi-coil transmitter**
- **Support precise 127.7kHz fixed frequency PA operation**
- **Integrated 32-bit ARM Cortex M0 processor**
- **Integrated 1M-bit NOR flash memory for program**
- **Bi-directional channel communication**
- **12-bit ADC for voltage/current measurement**
- **I2C programmable interface**
- **Foreign object detection**
- **Precise current sensor**
- **Over voltage protection**
- **Over current limit**
- **Over temperature protection**
- **Optional external power amp configuration**
- **128-bit One-Time-Programmable Device**
- **Low stand-by power**
- **QFN 48-pin 6mm x 6mm, 0.4mm pitch**

Applications

- Wireless charging pads
- Wireless power solutions for Mobile Applications

1. Description for Implementation

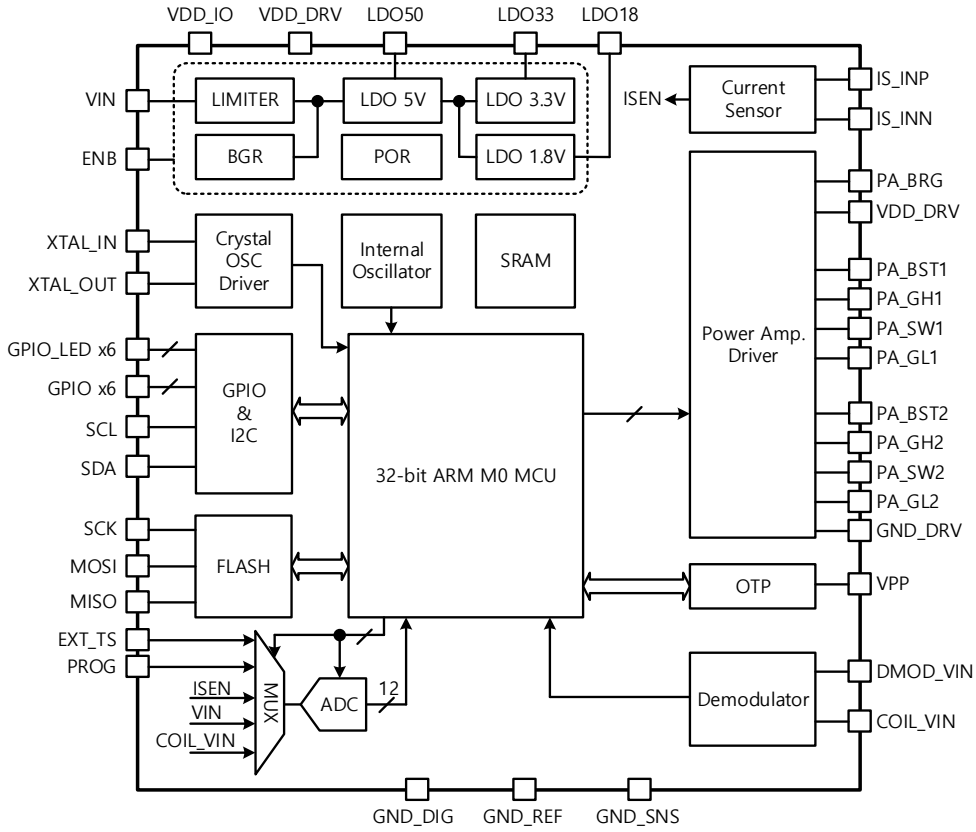

Figure 1. CWT2043 Block Diagram

1.1 Overview

A wireless power charging system is composed of transmitter and receiver. In general, wireless power transmitter will transfer AC power using a power amplifier through a TX inductor coil. Then wireless power receiver will receive AC power through an RX inductor coil which is strongly coupled with the TX coil. In transmitter part, power amplifier (PA) will change the DC power to AC power and transfer the AC power to the TX coil.

Figure1 shows the block diagram of CWT2043 wireless charging transmitter IC. CWT2043 transmitter will support power transfer up to 15W and it is compliant with WPC 1.2.4 standard. It consists of power amp driver, step down DC-DC converter, internal LDOs, ADC, 32-bit ARM M0 MCU, 1M-bit Flash memory, SRAM and etc.

1.2 Enable Pin and Start sequence

When the voltage on the ENB pin is pulled high, CWT2043 enters power down mode that is low current consumption. On the other hand, when the ENB pin is pulled low, CWT2043 is placed on active mode (power transfer mode or stand-by mode).

1.3 Crystal OSC Driver

CWT2043 employs an internal negative Gm driver in order to drive external crystal. CWT2043 can implement the precise power transfer frequency by using this crystal oscillator. Some applications often require accurate PA frequency implementation. With an external crystal, C

On the other hand, CWT2043 also supports the internal oscillator. For applications which do not require the correct frequency, we can lower the BOM by using the internal oscillator.

1.4 Power Amp Driver

The power amplifier of CWT2043 consists of four external power NLDMOSs and internal driver circuits. The power amp driver also includes boosting circuits for driving external high side NLDMOS. Each gate control signal can be adjusted by internal control and MCU.

The power amplifier of CWT2043 converts input DC power to AC power and transfers it directly to the TX coil. Since power amplifier directly influences the overall transmitter efficiency, the gate control of power MOSFET switches is very important. The power amp driver of CWT2043 changes its switching frequency and duty cycle according to the load current and feedback from the receiver.

1.5 FSK Modulator

The Qi extended power profile (EPP) uses two-way communication for power transfer. In the Qi standard, TX to RX communication is accomplished by frequency shift keying (FSK) modulation over the power signal frequency.

CWT2043 power transmitter uses FSK modulation for transmitting protocol data to the power receiver. CWT2043 changes the period of the power transfer signal by counting the internal 60MHz oscillator. The frequency deviation between the base operating frequency f_{OP} and the modulation frequency f_{MOD} is designed according to the Qi EPP standard.

1.6 ASK Demodulator

In the Qi standard, RX to TX communication is accomplished by amplitude shift keying (ASK) modulation with a bit rate of 2Kbps. CWT2043 power transmitter uses an external peak detection circuit and an internal comparator circuit for ASK demodulation. The external peak detection circuit include diode and filtering capacitors and resistors. The ASK demodulator in CWT2043 demodulates the WPC standard 2kHz bi-phase signal from the power receiver.

1.7 ADC

CWT2043 power transmitter employs 12-bit ADC because it has low power, small area characteristics and moderate speed performance. ADC monitors important internal voltages and currents and gives the system information to the digital controller.

1.8 Protection

CWT2043 power transmitter employs various protection schemes in order to prevent system damage. When the external power amplifier current is too large, the OCL (Over Current Limit) function will limit the output current. When the temperature inside or outside the chip is too high, the OTP (Over Temperature Protection) function will shut down the transmitter system to prevent damage resulting from excessive thermal stress under fault conditions.

1.9 Digital Controller

Digital controller of CWT2043 is composed of a 32-bit ARM Cortex M0 processor, 1M-bit Flash memory OTP, SRAM for program and data memory, etc. Digital controller controls all the analog blocks and entire system to perform power transfer operation according to the wireless power transfer Qi standard. CWT2043 supports the eight GPIO pins and two of them can be dedicated to I2C interface for communication with external host.

1.10 Current Sensor

CWT2043 includes the current sensor which is sensing at input current of external power amplifier with resistor of R_{SENS}. The value of sensing current (I_{SENS}) is decided below equation.

$$I_{SENS} = 50 \times R_{SENS} \times I_{PA}$$

Where, I_{SENS} is value of sensing current, I_{PA} is value of external power amplifier input current, and R_{SENS} is resistance of R_{SENS}.

2. Pin-out and description

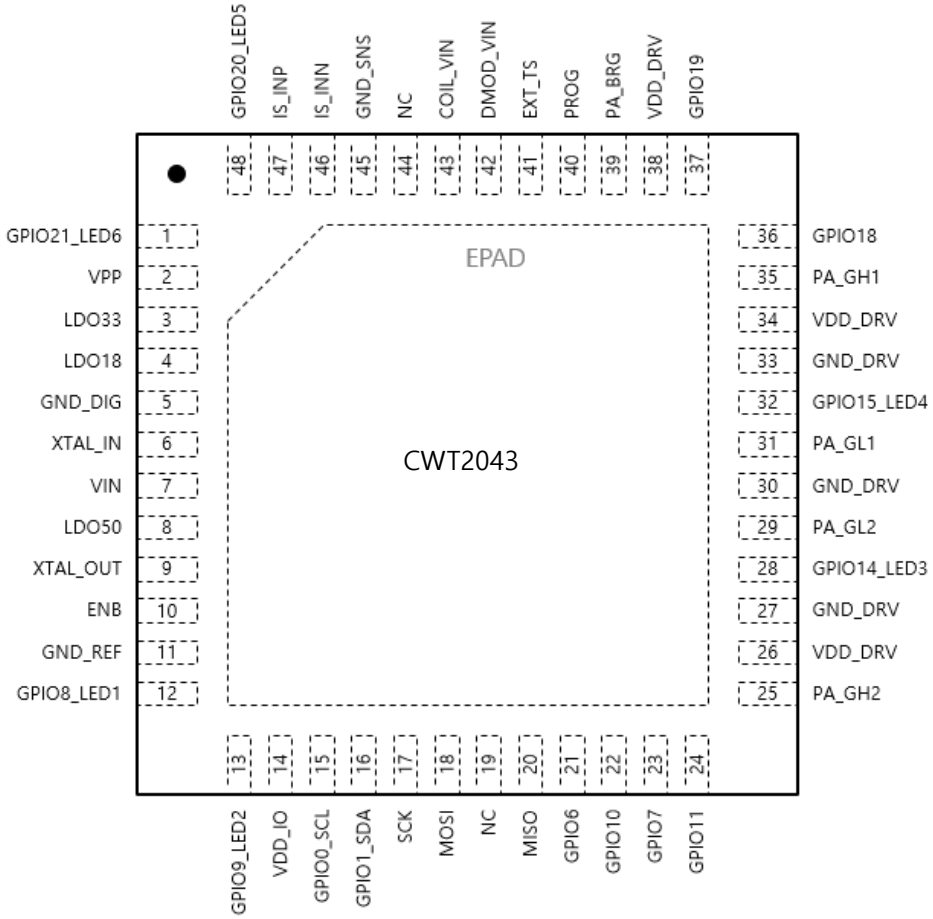

Figure 2. CWT2043 Pin Configuration (QFN 48-pin 6mm x 6mm, 0.4mm pitch)

2.1 Pin Description

Pin Number	Name	Type	Description
1 12 13 28 32 48	GPIO21_LED6 GPIO8_LED1 GPIO9_LED2 GPIO14_LED3 GPIO15_LED4 GPIO20_LED5	I/O	General purpose inputs/outputs. These pins can drive large pull-down current for high brightness LED applications.
2	VPP	I	8V high voltage power for OTP programming. During the normal operation, connect this pin to LDO33.
3	LDO33	O	Internal 3.3V LDO output pin for capacitor connection.
4	LDO18	O	Internal 1.8V LDO output pin for capacitor connection.
5	GND_DIG		Ground for internal digital block.
6	XTAL_IN	I	External crystal input
7	VIN	I	DC power input for power transmission.

8	LDO50	O	Internal 5V LDO output pin for capacitor connection.
9	XTAL_OUT	O	External crystal output
10	ENB	I	Active-low enable pin for the entire chip.
11	GND_REF		Ground for internal reference block.
14	VDD_IO	I	Input power supply for GPIO0~7. The operating range of this pin is 1.8~5.0V.
15	GPIO0_SCL	I/O	General purpose input/output 0. This pin can be dedicated for I^2C clock input for internal register access.
16	GPIO1_SDA	I/O	General purpose input/output 1. This pin can be dedicated for I^2C data input/output for internal register access.
17	SCK	O	Serial interface clock.
18	MOSI	I/O	Master data output. Slave data input. Multi TX communication
19	NC		Not connected
20	MISO	I/O	Master data input. Slave data output. Multi TX check
21 22 23 24 36 37	GPIO6 GPIO10 GPIO7 GPIO11 GPIO18 GPIO19	I/O	General purpose inputs/outputs
25	PA_GH2	O	PA gate driver output for the high side FET of half bridge 2.
26,34,38	VDD_DRV	I	Input power supply for the PA drivers.
27,30,33	GND_DRV		Ground for PA driver.
29	PA_GL2	O	PA gate driver output for the low side FET of half bridge 2.
31	PA_GL1	O	PA gate driver output for the low side FET of half bridge 1.
35	PA_GH1	O	PA gate driver output for the high side FET of half bridge 1.
39	PA_BRG	I	PA bridge voltage sensing pin.
40	PROG	I/O	I: Download ID pin and O: Debugging purpose
41	EXT_TS	I	External temperature sensor input. Connect this pin to external NTC thermistor. If not used, connect this pin to LDO33.
42	DMOD_VIN	I	Voltage sensing input pin for ASK demodulation.
43	COIL_VIN	I	Q factor Measurement
44	TEST_EN	I	FLASH SPI direct programming enable pin. (Internally pull-down) In the normal mode, this pin recommended N.C.
45	GND_SNS		Ground for internal sensors.
46	IS_INN	I	Input current sensor negative input.
47	IS_INP	I	Input current sensor positive input.
	EPAD		EPAD(Exposed PAD) pin must be connected to GND.

3. Application Guide

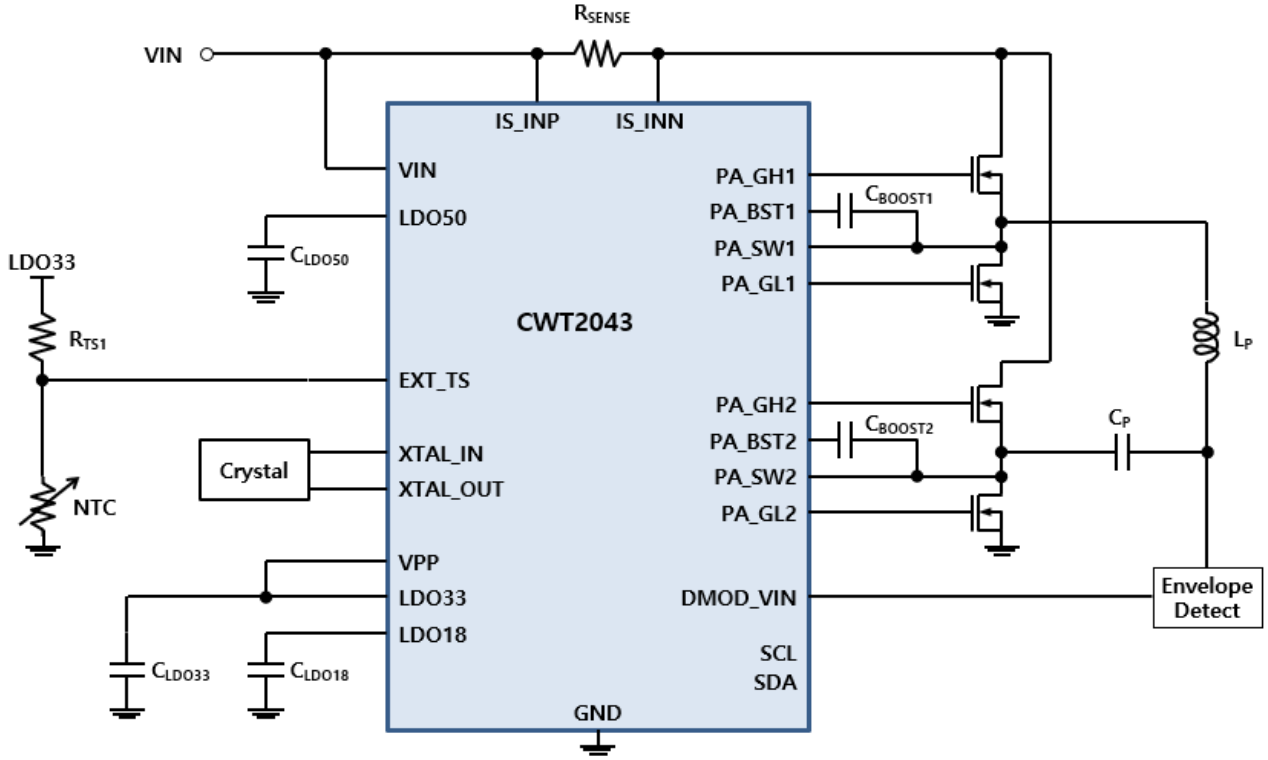

Figure 3. CWT2043 Typical Application Diagram

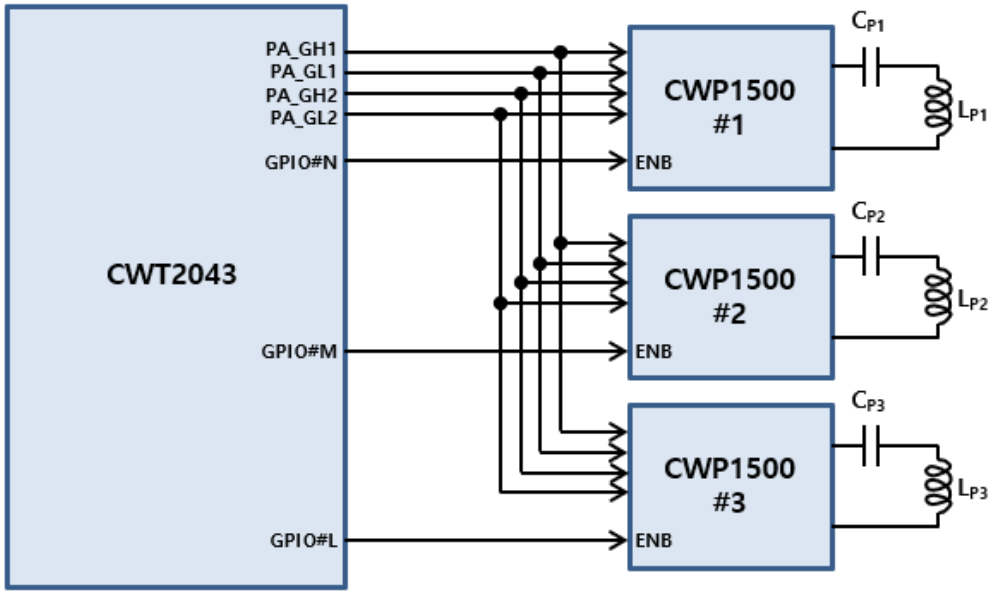

Figure 4. CWT2043 Multi-coil Application Diagram with CWP1500

3.1 Transmitter Coil and Resonant Capacitors

The transmitter coil design is related to the overall system application. The coil inductance, shape and material can be chosen according to its applications. However, it must comply with the WPC recommendations which include the self-inductance value, DC resistance, Q factor, etc. The resonant circuits of the power transmitter consist of an inductance L_P, a capacitance C_P, and a resistance R_P, where the R_P is the parasitic resistance. With respect to TX coil and capacitor, the resonant frequency f_P and the quality factor Q_P can be calculated by the following equations.

$$f_P = \frac{1}{2\pi\sqrt{L_P C_P}}$$

$$Q_P = \frac{2\pi f_P L_P}{R_P}$$

The resonant frequency f_P and the quality factor Q_P must be in the range of WPC recommendation.

3.2 Power MOSFETs and Boost Capacitors

As shown in Figure 3, CWT2043 power transmitter uses four external power MOSFETs for the power amplifier configuration. Since the input voltage range of CWT2043 is 0 to 20V, the external power MOSFETs should be high voltage devices. CWT2043 power transmitter uses two high side N-channel MOSFETs to improve efficiency and uses boosting circuits to drive them. The recommended power MOSFETs are 30V N-channel LDMOS.

As explained, two external bootstrap capacitors C_{BOOST1} and C_{BOOST2} are needed to drive the high-side FETs of external power amplifier. Bootstrap capacitors should have voltage rating of more than 25V and their recommended capacitances are 0.1uF.

3.3 Output Regulating Capacitors

As shown in Figure 3, internal LDOs' output LDO50, LDO33, LDO18 should be connected to external capacitor for voltage regulation. Typical recommended capacitance values are C_{LDO50}=1uF, C_{LDO33}=1uF, C_{LDO18}=1uF, respectively.

3.4 Input Current Sensing Resistor

The CWT2043 power transmitter uses an external resistor for the PA input current path to sense the input current. The sensing resistor tolerance should be less than 1% to meet the WPC FOD specification. Also, the current capacity of the resistor must be large because its maximum current reaches up to 2A.

3.5 External Temperature Sensor

When the temperature inside or outside the chip is too high, the OTP (Over Temperature Protection) function will send the EPT packet to transmitter or shutdown the receiver system. In order to sense the temperature outside chip, connect EXT_TS pin to external NTC (Negative temperature Coefficient) thermistor as shown in Figure 3. The NTC thermistor should be placed close to the heat emission device.

The EXT_TS voltage V_{EXT_TS} can be calculated as follows,

$$V_{EXT\_TS} = V_{LDO33} \times \frac{R_{NTC}}{R_{TS1} + R_{NTC}}$$

In this equation, V_{LDO33} is 3.3V from the internal LDO.

The MCU in the CWT2043 compares the quantitative value of V_{EXT_TS} which are generated by ADC with programmable internal reference values. After choosing the appropriate NTC thermistor, you can design R_{TS1} and R_{NTC} according to your thermal protection specification. Table 1 shows the EXT_TS thermal protection design example. In this example, the hot temperature threshold is designed to be 70℃. You can change the hot temperature threshold according to your application by changing the R_{TS1} resistor.

Table 1. EXT_TS Thermal Protection Design Example

Temp [℃]	V_{LDO33} [V]	R_{NTC} [kΩ]	R_{TS1} [kΩ]	V_{TS_EOC} [V]	ADC_Val [Dec.]	Status
20	3.3	12.50	15	1.500	3413	Normal case
30	3.3	8.05	15	1.152	2623	
40	3.3	5.32	15	0.863	1965	
50	3.3	3.59	15	0.637	1450	
60	3.3	2.48	15	0.467	1064	
70	3.3	1.74	15	0.343	781	End Power Transfer
80	3.3	1.25	15	0.253	576	
90	3.3	0.91	15	0.188	429	

3.6 PCB Layout Guide

- Keep the trace resistance as low as possible on large current nets associated with the external power MOSFETs.
- Resonant capacitor C_P needs to be as close to the device as possible.
- Boost capacitors (C_{BOOST1}, C_{BOOST2}) need to be as close to the device as possible.
- Output regulating capacitors C_{LDO_IN}, C_{LDO50}, C_{LDO33} and C_{LDO18} need to be as close to the device as possible.

4. Package Outline

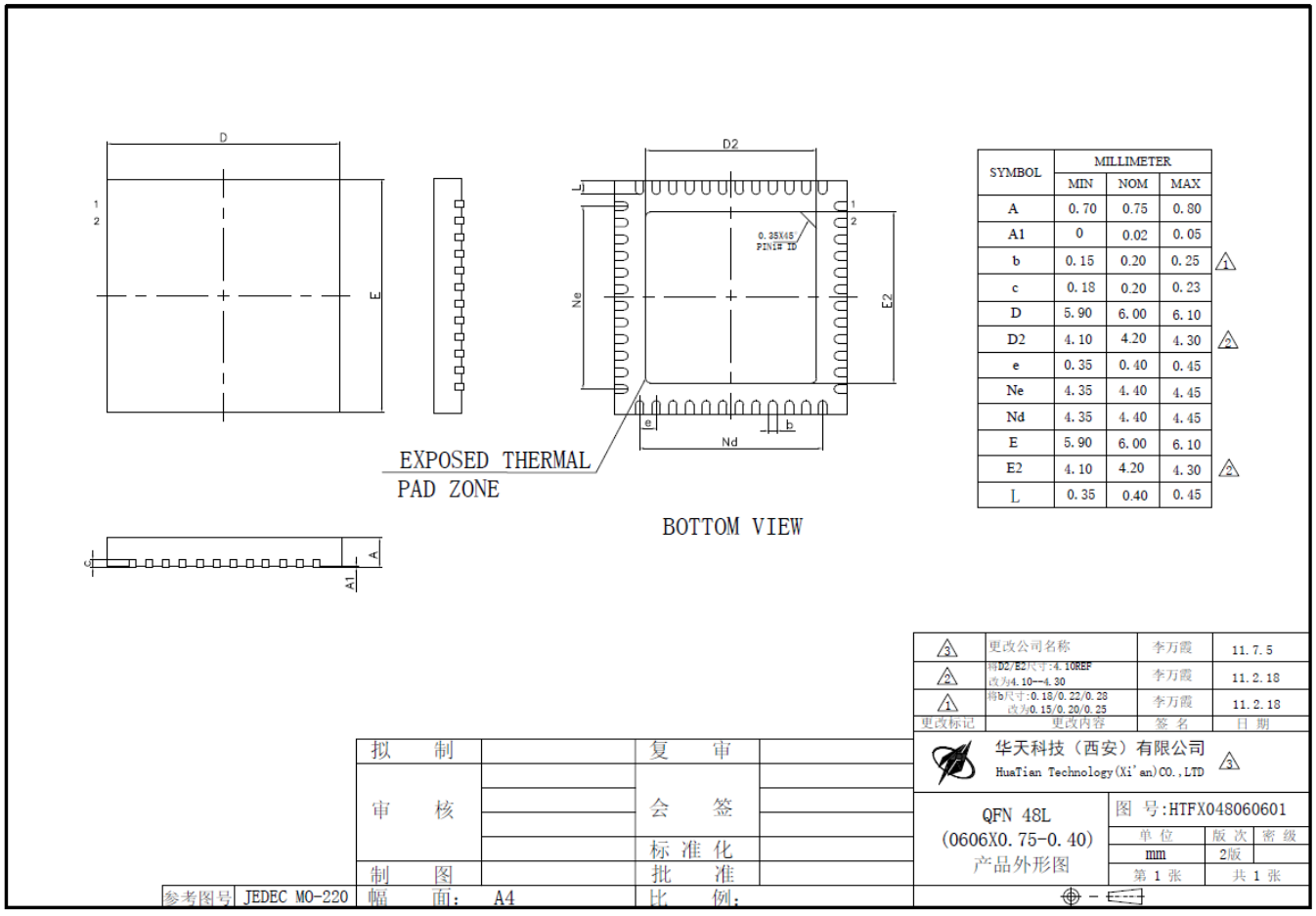

Figure 5. QFN 48-pin Package Outline, 6.0mm x 6.0mm, 0.4mm pitch

5. Electrical Characteristics

5.1 Absolute Maximum Rating

PIN	Parameter	Rating	Unit
VIN, ENB, PA_GH2, PA_BST2 PA_SW2, PA_SW1, PA_BST1, PA_GH1, PA_BRG IS_INP, IS_INN	Voltage	-0.3 to 24	V
VPP	Voltage	-0.3 to 8	V
LDO33, LDO50, PA_GL2, PA_GL1, VDD_DRV, PROG, EXT_TS, DMOD_VIN, COIL_VIN, TEST_EN	Voltage	-0.3 to 6	V
VDD_IO, GPIO0_SCL, GPIO1_SDA, SCK, MOSI, MISO, GPIO21_LED6, GPIO8_LED1, GPIO9_LED2, GPIO14_LED3, GPIO15_LED4, GPIO20_LED5, GPIO6, GPIO10, GPIO7, GPIO11, GPIO18, GPIO19, FLASH_CSN	Voltage	-0.3 to 4	V
LDO18, XTAL_IN, XTAL_OUT	Voltage	-0.3 to 2	V
GND_DIG, GND_REF, GND_SNS, GND_DRV	Voltage	-0.3 to 0.3	V

5.2 Recommended Operating Condition

Symbol	Description	Min.	Typ.	Max.	Unit
V_{IN}	DC power input for power transmission.	4.5		20.0	V
T_J	Junction temperature	-40		125	℃
T_A	Ambient temperature	-40		85	℃

5.3 Device Characteristics

Symbol	Description	Conditions	Min.	Typ.	Max.	Unit
Input Supply and Current Consumption						
V_{IN}	Input supply voltage range		4.5		20.0	V
V_{UVLO}	Under voltage lockout (V_{UVLO_F})	V_{IN}: 4.60V to 3.90V	4.05	4.2	4.35	V
	Under voltage lockout (V_{UVLO_R})	V_{IN}: 3.90V to 4.60V	4.15	4.3	4.45	V
V_{UVLO_HYS}	Under voltage lockout hysteresis	V_{IN}: 5V to 0V	25	200	400	mV
I_{ACTIVE}	Input current at power transfer mode	V_{IN}=12V		7.5		mA
I_{IDLE}	Input current at stand-by mode (periodic ping)	V_{IN}=12V		5		mA
I_{SHD}	Input current at power down mode	ENB=V_{IN}=12V		46		uA
Power Amplifier and Driver						

f_{PA}	Power amplifier switching frequency		85	127.7	205	kHz
T_{LS_SW}	Low side gate driver rising and falling times			90	150	ns
T_{HS_SW}	High side gate driver rising and falling times			100	300	ns
$P_{OUT\_PA\_MAX}$	Power amplifier maximum output power			15		W
Internal LDOs						
V_{OUT_LDO50}	Internal LDO50 output voltage range	V_{IN}>5V	4.85	5	5.15	V
$I_{OUT\_LDO50\_MAX}$	LDO50 maximum output current				20	mA
V_{OUT_LDO33}	Internal LDO33 output voltage range	V_{IN}>5V	3.2	3.3	3.4	V
$I_{OUT\_LDO33\_MAX}$	LDO33 maximum output current				20	mA
V_{OUT_LDO18}	Internal LDO18 output voltage range	V_{IN}>5V	1.67	1.8	1.94	V
$I_{OUT\_LDO18\_MAX}$	LDO18 maximum output current				10	mA
Internal Oscillators						
f_{OSC60M}	Internal main oscillator frequency Register programmable	V_{IN}>3.3V	58.2	60	61.8	MHz
ADC						
N_{ADC}	ADC resolution	V_{IN}>3.3V		12		bit
f_{SAMPLE}	ADC sampling rate	f_{OSC60M}=60MHz	210	217	224	kSa/s
N_{CH_ADC}	ADC channel			8		
Protection						
I_{OCL}	I_{IN} over current limit protection	R_{SENSE}=20mΩ		2	2.15	A
T_{OTP}	Over temperature protection Thermal shutdown temperature	Temperature: 30℃ to 160℃		150		℃
T_{OTP_HYS}	OTP hysteresis	Temperature: 160℃ to 30℃		20		℃
V_{TS_HOT}	EXT_TS hot temperature protection detection temperature	Temperature: 30℃ to 80℃		70		℃
$V_{TS\_HOT\_HYS}$	EXT_TS hot temperature protection release temperature	Temperature: 80℃ to 30℃		60		℃

6. I²C Signal Timing

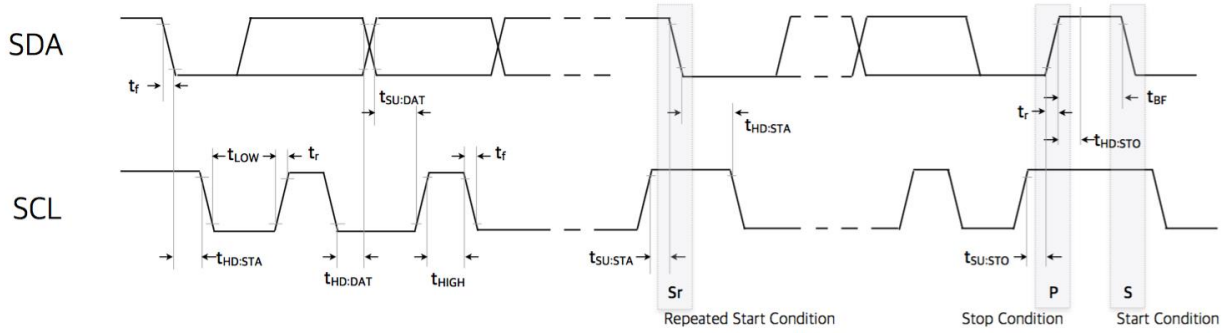

Figure 6. Timing Diagram for I²C interface

Symbol	Description	Conditions	Min.	Typ.	Max.	Unit
V_{IL_SDA}	Input low threshold level SDA	V_{PULLUP}=VDD_IO=3.3V			0.7	V
V_{IH_SDA}	Input high threshold level SDA	V_{PULLUP}=VDD_IO=3.3V	2.6			V
V_{IL_SCL}	Input low threshold level SCL	V_{PULLUP}=VDD_IO=3.3V			0.7	V
V_{IH_SCL}	Input high threshold level SCL	V_{PULLUP}=VDD_IO=3.3V	2.6			V
f_{SCL}	SCL clock frequency				400	kHz
t_{LOW}	SCL clock low time		1.3			us
t_{HIGH}	SCL clock high time		0.6			us
t_r	Rise time of both SDA and SCL				0.3	us
t_f	Fall time of both SDA and SCL				0.3	us
$t_{SU,STA}$	Setup time for START condition		0.6			us
$t_{HD,STA}$	Hold time for START condition		0.6			us
$t_{SU,DAT}$	Data setup time		0.1			us
$t_{HD,DAT}$	Data hold time				0.9	us
$t_{SU,STO}$	Setup time for STOP condition		0.6			us
t_{BF}	Bus free time between STOP and START condition		1.3			us

Table 2. I²C Characteristics

Revision History

Date	Version No.	Description
2020/03/09	1.0	Preliminary Release

Ordering Information

Part Number	Package Type	Shipping Carrier	Package Qty	Eco Plan	MSL Peak Temp	Description	Device Marking
CWT2043	QFN 48pin, 6.0mm x 6.0mm	Tape and Reel	4,000	Green (RoHS&noSb/Br)	Level-3-260C-UNLIM	15W Fixed-Frequency Solution	AJ