CWR510Q® Datasheet

Qi Compliant 5W
Wireless Power Receiver IC

General Description

CWR510Q can deliver up to 5W as a highly-integrated single-chip wireless medium power receiver IC. As wireless power transfer systems are getting more popular, they require more faster charging and higher efficiency solution. The CWR510Q wireless power receiver IC is compliant with WPC 1.2.4 standard and supports the 5W baseband power profile (BPP). The CWR510Q power receiver integrates a synchronous rectifier, a low drop-out regulator, and communication controllers which use Amplitude Shift Keying (ASK). CWR510Q includes a 32-bit ARM Cortex M0 processor in order to offer high level of programmability according to its applications and it also supports the Foreign Object Detection (FOD) extension in WPC 1.2.4. For achieving chip stability, protection tools are implemented, such as over-current-protection, over-voltage-protection, thermal shutdown, and under voltage lock-out (UVLO). Configurable analog blocks can be used independently and co-operated with the control and communication unit.

Features Overview

- **Single-chip dual mode 5W receiver for WPC 1.2.4 compliance**
  - WPC 1.2.4 TPT#MP1 (5W)
- **Support 5W baseline power profile (BPP)**
- **FOD extension supports**
- **Integrated Synchronous Rectifier Receiver.**
  - Support Output Power up to 5W.
  - High Rectifier Efficiency up to 95%.
  - High System Efficiency up to 90%.
  - Topology Auto Selection operation.
- **Programmable Dynamic Rectifier Voltage Control.**
- **Integrated Programmable Linear Regulator.**
  - Output voltage range of 3.5~7V with 20mV control step.
  - Output current up to 1A @ 7V
- Integrated 32-bit ARM Cortex M0 processor
  - Integrated MTP for program memory
  - Integrated SRAM for data memory
- Bi-directional channel communication
  - ASK modulation for PRx to PTx
- **24-bit Power Calculation support**
- **Received Power Calculation for FOD function**
  - 12-bit ADC for voltage/current measurement.
  - Adaptive Coil Power loss/offset compensation.
- **Programmable Temperature Control.**
- **Transmit Coil and Receive Coil Alignment**
- **Charger Complete and Enable control inputs**
- **End of Power Transfer (EPT) Packet management.**
- **Over Current Limit**
- **Over Voltage Protection**
- **Thermal Shutdown**
- **QFN 40pin 6.00mm x 6.00mm, 0.5mm pitch**

Applications

- WPC Compliant 5W Receivers.
- Power Banks.
- Wireless Power Embedded Batteries
- Bluetooth Headsets
- Smart Watch and TWS earphone applications
- Portable Media Players
- Other Hand-held Device

1. Description for Implementation

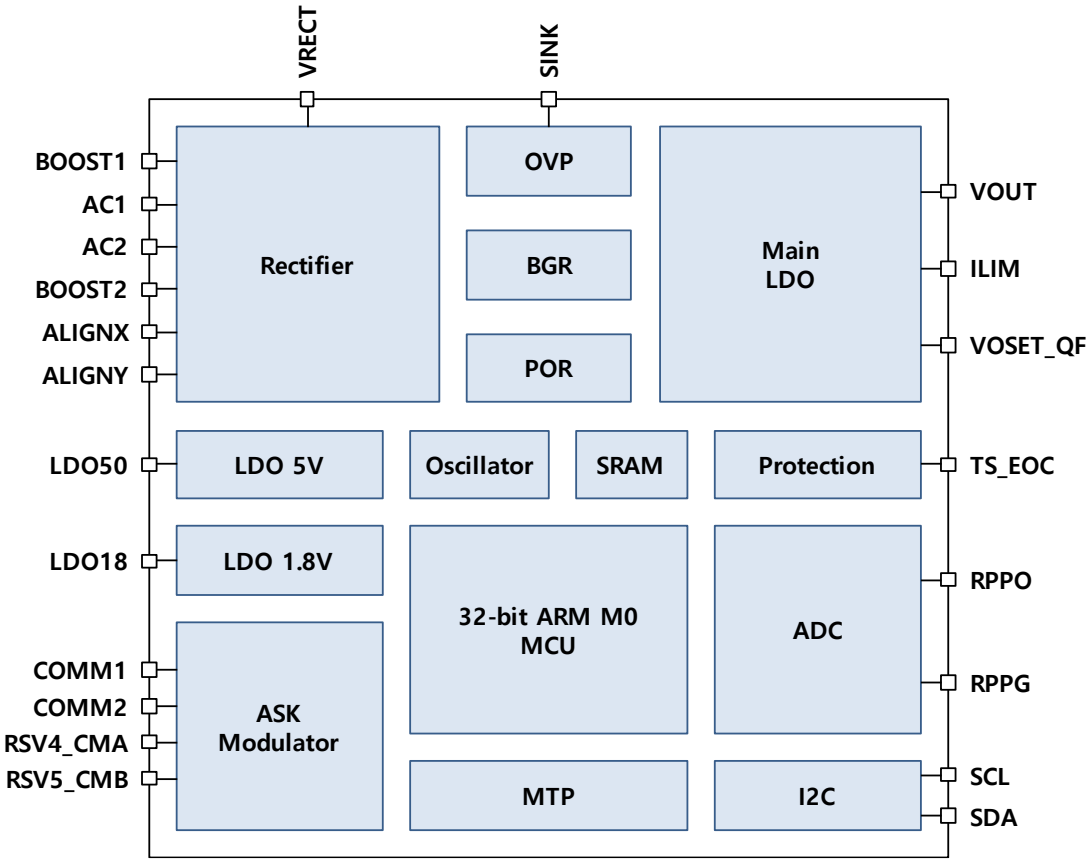


Figure 1. CWR510Q Block Diagram

1.1 Overview

A wireless power charging system is composed of transmitter and receiver. In general, wireless power transmitter will transfer AC power using a power amplifier through a TX inductor coil. Then wireless power receiver will receive AC power through an RX inductor coil which is strongly coupled with the TX coil. In receiver part, rectifier will change the AC power to DC power and Main LDO will transfer the DC power to battery charger.

Figure 1. shows the block diagram of CWR510Q wireless charging receiver IC. CWR510Q receiver will support power transfer up to 5W and it is compliant with WPC1.2.4 standards. It consists of rectifier, Main LDO, internal LDOs, ADC, ASK modulator, 32-bit ARM M0 MCU, MTP, SRAM, etc.

1.2 Rectifier

CWR510Q employs a synchronous active rectifier in order to improve AC to DC power conversion efficiency. The rectifier power conversion efficiency is very important because it has a large influence on overall receiver efficiency. The rectifier in CWR510Q will support full-wave, half-wave and passive mode according to the transferred power level. When the power transfer is started initially, the rectifier will operate in passive mode and supply the system power to overall receive IC.

1.3 Main LDO

Main LDO regulator will transfer DC power from rectifier output to battery charger. LDO in CWR510Q is designed to transfer power up to 5W and its output voltage can be set by user. The output voltage range is 3.5 V to 7.0 V and set the output voltage (VOUT) by either the internal register bits or external resistors (R_{VOSET1} and R_{VOSET2}). The LDO power transistor is designed to minimize its on-resistance because the LDO drop-out voltage is directly related to overall system efficiency. Especially, in case of large power transfer, the LDO drop-out voltage (VRECT-VOUT) should be controlled as small as possible. The Main LDO has the feature of protection that is programmable over current limit (OVP). The OVP protect the Main LDO circuit in the CWR510Q, and external devices on the VOUT node from over current.

1.4 ASK Modulator

CWR510Q power receiver communicates with the power transmitter by ASK modulator. The ASK modulator makes up the WPC standard 2kHz bi-phase signal by switching the capacitors between COMM1/2 and AC1/AC2. Switching the capacitance at AC1/AC2 nodes will change the impedance of transmitter coil. As a result, amplitude modulation is built up.

1.5 ADC

CWR510Q power receiver employs 12-bit SAR ADC because it has low power, small area characteristics and moderate speed performance. ADC monitors important internal voltages and currents and gives the system information to the digital controller.

1.6 Protection

CWR510Q power receiver employs various protection schemes in order to prevent system damage. When the VRECT voltage is too high, the OVP (Over Voltage Protection) function will turn on the clamp path or send the EPT (End Power Transfer) packet to the transmitter. When the Main LDO current is too large, the OCL (Over Current Limit) function will limit the output current. When the temperature inside or outside the chip is too high, the OTP (Over Temperature Protection) function will send the EPT packet to transmitter or shutdown the receiver system.

1.7 Digital Controller

Digital controller of CWR510Q is composed of a 32-bit ARM Cortex M0 processor, MTP, SRAM for program and data memory, etc. The digital controller controls all the analog blocks and entire system to perform power transfer operation according to the wireless power transfer standard, that is, WPC 1.2.4. CWR510Q supports I^2C interface to communicate with external host.

2. Pin-out and description

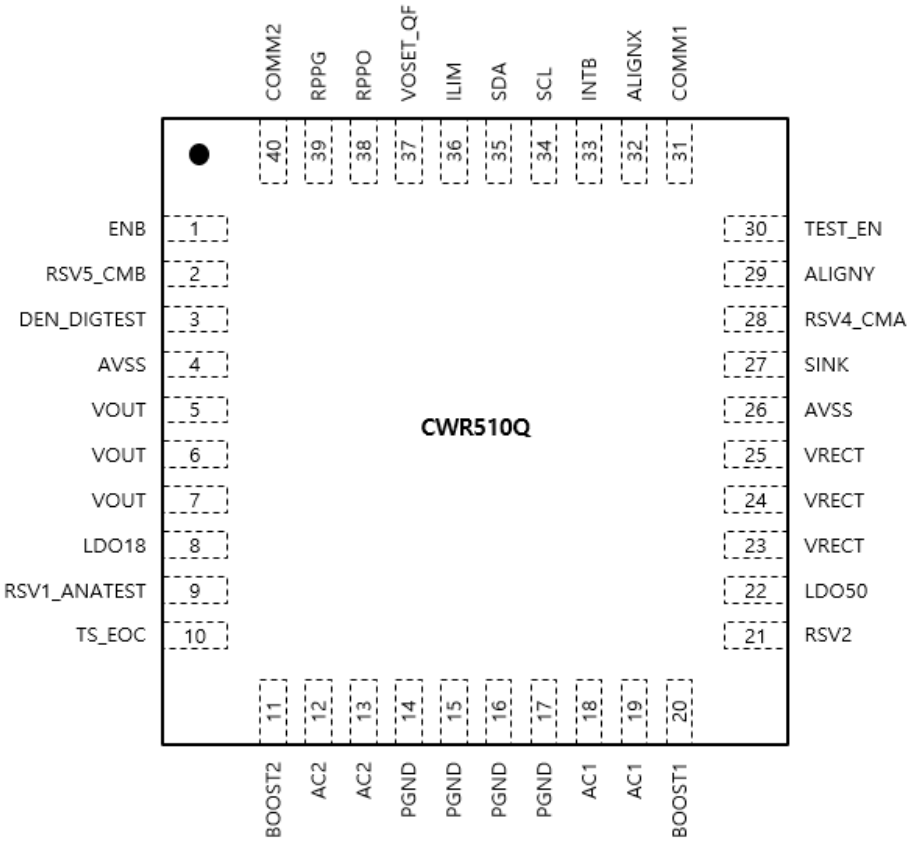


Figure 2. CWR510Q Pin Configuration (QFN 40pin, 6.00mm x 6.00mm, 0.5mm pitch)

2.1 Pin Description (QFN 40pin, 6.00mm x 6.00mm, 0.5mm pitch)

Pin Number	Name	Type	Description
31	COMM1	O	High voltage open drain output for ASK modulation. Connect 22nF capacitor from AC1/AC2 to COMM1/COMM2 respectively.
40	COMM2	O	
32	ALIGNX	I	AC input for coil alignment guide. If this function is not used, connect to GND through a 10kΩ resistor.
34	SCL	I	I^2C clock input for internal register access.
37	VOSET_QF	I	Programming pin for setting the VOUT voltage. Connect VOSET pin to the center tap of the resistor divider to set the VOUT voltage.
39	RPPG	I	Received power packet gain (RPPG) calibration pin for FOD tuning. This pin should be connected to the center tap of the resistor divider to set the gain of the FOD. If this pin is connected to half of LDO18 voltage, RPPG calibration is disable.
28	RSV4_CMA	O	High voltage open drain output for ASK modulation. Connect a 22nF capacitor from AC1/AC2 to RSV4_CMA/RSV5_CMB respectively.
2	RSV5_CMB	O	

29	ALIGNY	I	AC input for coil alignment guide. If this function is not used, connect to GND through a 10kΩ resistor.
35	SDA	I/O	I^2C data input/output for internal register access.
30	TEST_EN	I	Scan test enable pin
36	ILIM	I	Over-current limit level programming pin.
1	ENB	I	Active-low enable pin for the entire chip.
4, 26	AVSS	GND	Analog ground pin.
27	SINK	O	Open drain output pin to control the voltage of VRECT. Connect to the resistor from SINK pin to VRECT pin.
33	INTB	I/O	GPIO type, active low interrupt flag pin. When the fault condition is detected, it is pulled low. The fault conditions are as follows: OVP, OCP, TSD_HOT, ENB=high
38	RPPO	I	Received power packet offset (RPPO) calibration pin. This pin should be connected to the center tap of the resistor divider to set the offset of the FOD. If this pin is connected to half of LDO18 voltage, RPPO calibration is disable.
3	DEN_DIGTEST	O	Digital test output pin. Floating for normal application
5,6,7	VOUT	O	Main LDO output pin for delivering power to the battery charger. Connect two 10uF capacitor to GND.
23,24,25	VRECT	O	Internal synchronous rectifier output. Connect three 10uF capacitor to GND.
22	LDO50	O	Internal 5V LDO output pin. Connect a 1uF capacitor from LDO50 pin to GND. Not for external use.
8	LDO18	O	Internal 1.8V LDO output. Connect a 1uF capacitor from LDO18 pin to GND. Not for external use.
20	BOOST1	O	Bootstrap capacitor connection pin for driving the high-side FETs of synchronous rectifier. Connect a 22nF capacitor to AC1/AC2 respectively.
11	BOOST2	O	
9	RSV1_ANA_TEST	O	Analog test output pin. Floating for normal application
18, 19	AC1	I	AC power input of synchronous rectifier.
12,13	AC2	I	
21	RSV2	-	Reserved pin. This pin can be connected to GND or VOUT, when it is not used
10	TS_EOC	I	External temperature sensor input. Connect this pin to external NTC thermistor. If not used, connect this pin to LDO18.
14,15,16,17	PGND	GND	Power ground for synchronous rectifier.

3. Application Guide

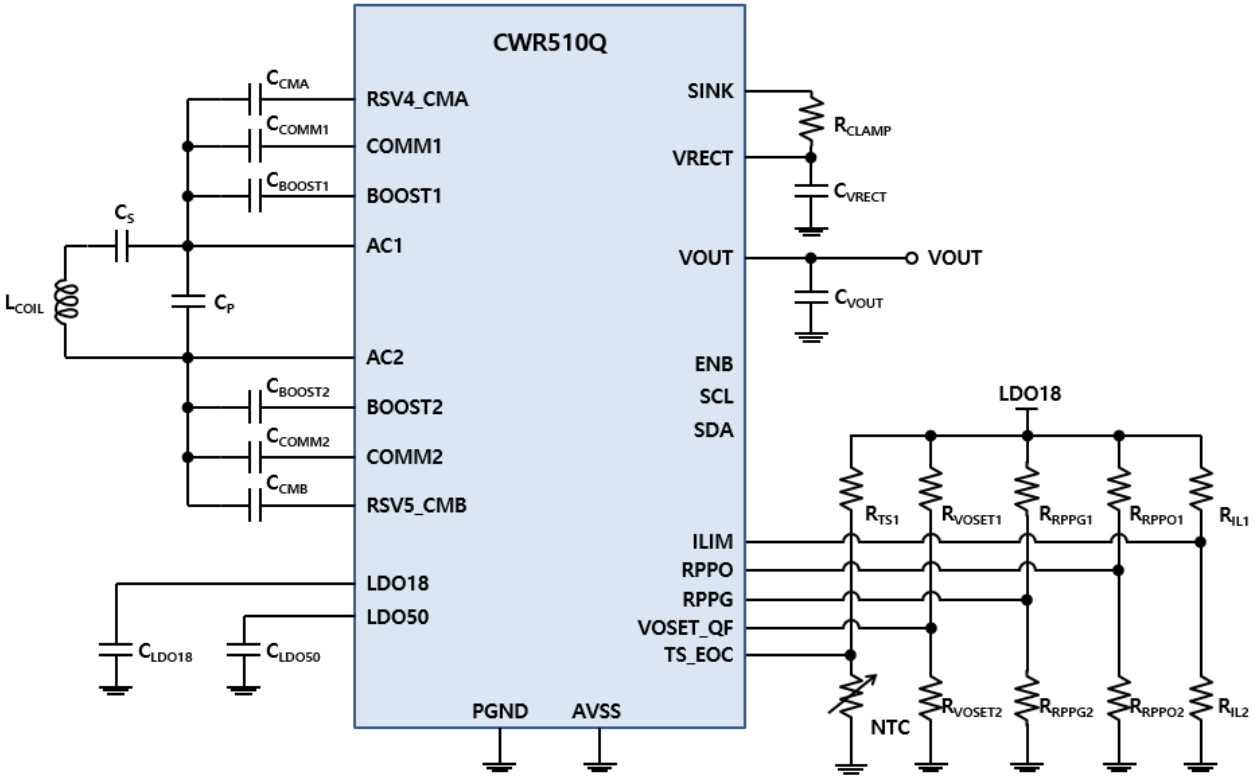


Figure 3. CWR510Q Typical Application Diagram

3.1 Receiver Coil and Resonant Capacitors

The receiver coil design is related to the overall system application. The coil inductance, shape and material can be chosen according to the applications. The recommended receiver coil inductance for dual mode operation is between 5uH to 10uH. Series and parallel resonant capacitors C_S and C_d are set according to WPC specification. The capacitance of the resonant capacitors can be calculated by the following equations.

$$C_S = \frac{1}{L'_S \times (2\pi f_S)^2}$$

$$C_d = \frac{1}{L_S \times (2\pi f_D)^2 - \frac{1}{C_S}}$$

In these equations, f_S and f_D are the dual resonant frequencies which cover the power transfer frequency range. Follow WPC Qi 1.2.4 specifications, f_S is set to 100 kHz and f_D is set to 1000kHz, respectively. L'_S is coil self-inductance when placed on the transmitter, and L_S is the self-inductance when placed away from the transmitter.

3.2 Boost and Communication Capacitors

As shown in Figure 4, two external bootstrap capacitors C_{BOOST1} and C_{BOOST2} are needed to drive the high-side FETs of synchronous rectifier. Bootstrap capacitors should have voltage rating of more than 16V and their recommended capacitances are 22nF.

In order to communicate with transmitter, external capacitors should be connected between high voltage open drain output and AC1/AC2 input. CWR510Q will be switching COMM1/COMM2 output in WPC mode. Typical recommended capacitance values are C_{COMM1}=C_{COMM2}= C_{CMA}= C_{CMB}=22nF.

3.3 Output Regulating Capacitors

As shown in Figure 4, rectifier output VRECT and internal LDOs' output VOUT, LDO50, LDO18 should be connected to external capacitor for voltage regulation. Typical recommended capacitance values are C_{VRECT}=30uF, C_{VOUT}=20uF, C_{LDO50}=1uF, C_{LDO18}=1uF, respectively.

3.4 Clamp Resistor

When the VRECT voltage is too high, the OVP (Over Voltage Protection) function will turn on the clamp path or send the EPT (End Power Transfer) packet to the transmitter. The clamp path uses high voltage open drain output for analog linear OVP. The recommended resistance value of R_{CLAMP} is between 10Ω to 50Ω according to the transfer power level of application.

3.5 Over Current Limit

When the Main LDO current is too large, the OCL (Over Current Limit) function will limit the output current. The current limit level can be adjusted by external resistors and it is calculated as follows,

$$I_{OCL} = V_{ILIM} \times 1.167$$

where, I_{OCL} is the setting value of over current limit, V_{ILIM} is the voltage of ILIM pin. The V_{ILIM} is generated by R_{IL1} and R_{IL2} as shown in the Figure 4. It is recommended to set I_{OCL} to 120% of the target maximum output current. The table1 shows the reference value of R_{IL1} and R_{IL2} for over current limit.

Table 1. Setting the Over Current Limit

R_{IL1} [kΩ]	R_{IL2} [kΩ]	IOUT [A]	I_{OCL} [A]
10	Open	1.8	2.1
10	32	1.25	1.6
10	10	0.80	1.0
10	6.2	0.64	0.8
10	3.2	0.40	0.5

3.6 Received Power Packet Offset (RPPO) and Received Power Packet Gain (RPPG)

CWR510Q has the FOD calibration functions which can calibrate received power by offset and gain proportional to output power level when it sends the received power packet to the transmitter. The ratio of the R_{RPPG1} and R_{RPPG2} set the gain of the RPPG function. Also, the ratio of the R_{RPPO1} and R_{PPO2} set the received power offset for FOD.

The received power packet offset (RPPO) and received power packet gain (RPPG) calibrations utilize dedicated pins for tuning foreign object detection (FOD). These calibrations tune the received power packet via the voltage levels on the RPPO and RPPG pins, which are determined by the external resistors in divider networks on the 1.8V bias voltage. The voltage level on the RPPO pin is used to add offset in order to shift the Received Power Packet (RPP) globally, and the voltage level on the RPPG pin adjusts the slope gain of the Received Power Packet (RPP).

- The received power packet offset calibration can be tuned by varying the voltage on the RPPO pin from 0.1V to 1.8V corresponding to a power offset range from 55mW to 1000mW.
- The received power packet gain can be tuned by varying the voltage on the RPPG pin from 0.1V to 1.8V corresponding to a gain setting in the range from 0.111 to 1.999.
- To disable the FOD, the RPP0 and RPPG must be connected to GND.

The RPP is adjusted according to Equation 2:

$$RPP[mW] = P_{measured}[mW] \times \frac{RPPG}{2048}[\%] + P_{LOSS}[mW] \times \frac{RPPO}{2048}[\%] \quad \text{Equation 2}$$

Where

RPP = Received Power Packet

$P_{measured}$ = measured power from output voltage and current

P_{LOSS} = Power receiver power consumption and magnetic field loss

$$RPPO = \frac{V_{RPPO}[V]}{1.8[V]} \times 4095 \quad \text{Equation 3}$$

$$RPPG = \frac{V_{RPPG}[V]}{1.8[V]} \times 4095 \quad \text{Equation 4}$$

3.7 Output Voltage Setting (VOSET_QF)

The CWR510Q has two methods for setting of output voltage. First method, the output voltage (VOUT) of the CWR510Q is programmed by voltage of the VOSET_QF pin that is set the external resistors R_{VOSET1} and R_{VOSET2} as shown in Figure 4.

Table 2. Setting the VOUT (Output voltage)

R_{VOSET1} [kΩ]	R_{VOSET2} [kΩ]	VOUT [V]	5 V Operation
10	Open	12	Enable
10	>21	12	Enable
10	0.31k<R_{VOSET2}< 4.9k	9	Enable
OPEN	10	5	Enable
10	<0.3	5	Enable

3.8 External Temperature Sensor

When the temperature inside or outside the chip is too high, the OTP (Over Temperature Protection) function will send the EPT packet to transmitter or shutdown the receiver system. In order to sense the temperature outside chip, connect TS_EOC pin to external NTC (Negative temperature Coefficient) thermistor as shown in Figure 4. The NTC thermistor should be placed close to the heat emission device.

The TS_EOC voltage V_{TS_EOC} can be calculated as follows,

$$V_{TS\_EOC} = LDO18 \times \frac{R_{NTC}}{R_{NTC} + R_{TS1}}$$

In this equation, LDO18 is 1.8V from the internal LDO.

The MCU in the CWR510Q compares the quantitative value of V_{TS_EOC} which are generated by ADC with programmable internal reference values.

Recommended NTC resistance (R_{NTC}) range is from hundreds of ohm to hundreds of kilo-ohm depending on the temperature. After choosing the appropriate NTC thermistor, you can design R_{TS1} and R_{NTC} according to your thermal protection specification. Table 3 shows a TS_EOC thermal protection design example. In this example, the hot temperature threshold is designed to be 70℃. You can change the hot temperature threshold according to your application by changing the related resistors.

Table 3. TS_EOC Thermal Protection Design Example

Temp [℃]	LDO18 [V]	R_{NTC} [kΩ]	R_{TS1} [kΩ]	V_{TS_EOC} [V]	ADC_Val [Dec.]	Status
0	1.8	32.7	4.7	1.574	3581	Normal charging operation (Only use the OTP hot)
10	1.8	19.93	4.7	1.457	3314	
20	1.8	12.50	4.7	1.308	2977	
30	1.8	8.05	4.7	1.136	2586	
40	1.8	5.32	4.7	0.955	2174	
50	1.8	3.59	4.7	0.779	1774	
60	1.8	2.48	4.7	0.621	1413	
70	1.8	1.74	4.7	0.487	1107	Send EPT packet
80	1.8	1.25	4.7	0.377	859	
90	1.8	0.91	4.7	0.292	664	

3.9 End of Charge

When the voltage of TS_EOC pin is less than 0.1V, state of CWR510Q becomes the End of Charge (EOC). When the state of CWR510Q is EOC, CWR510Q will send the End Power Transfer (EPT) packet to the transmitter and the transmitter will terminate the delivery power.

3.10 ENB

When applying logic high to ENB, CWR510Q is suspended and IC leakage current will be smaller than 10uA. When ENB is logic low level, CWR510Q is enabled for wireless charging.

3.11 Alignment Guide (ALIGNX and ALIGNY)

The CWR510Q has the coil alignment feature that gives the information the transmit coil and receive coil alignment during the normal operation. The alignment function in the CWR510Q provide quantitative information on the amount misalignment. That the values of quantitative information (ALIGNX and ALIGNY) are higher is more the coils are misaligned.

3.12 PCB Layout Guide

- Keep the trace resistance as low as possible on large current nets as shown in Table 4.
- Resonant capacitors C_S and C_d need to be as close to the device as possible.
- Clamp, boost and communication capacitors (C_{BOOST1}, C_{BOOST2}, C_{COMM1}, and C_{COMM2}) need to be as close to the device as possible.
- Output regulating capacitors C_{VRECT} and C_{VOUT} need to be as close to the device as possible.

Table 4. Large Current Nets

Net (Ball)	Type	Maximum Current [A]
AC1, AC2	AC	2
VRECT	AC	2
VOUT	DC	2
PGND	AC	2
COMM1, COMM2	AC	1
SINK	AC	2

3.13 Register Map

The following tables provide the address locations, field names, available operations (R or RW), default values, and functional descriptions of all the internally accessible registers contained within the CWR510Q. The default I²C slave address is 24H. The address of each register has a two-byte structure. For example, the low byte of major firmware revision must be read with two bytes address with 00HEX and 04HEX.

Table 5. Read Register – Device Identification Register

REG	Bit	Field	Type	Default	Description
0000_{HEX}	**7:0**	Part_number_L	R	0x00	slave device address low byte
0000_{HEX}	**7:0**	Part_number_H	R	0x20	slave device address high byte

Table 6. Read Register – Firmware Major Revision

REG	Bit	Field	Type	Default	Description
0004_{HEX}	**7:0**	FW_Major_Rev_L	R	0x01	Major firmware revision low byte
0005_{HEX}	**7:0**	FW_Major_Rev_H	R	0x00	Major firmware revision high byte

Table 7. Read Register – Firmware Minor Revision

REG	Bit	Field	Type	Default	Description
0006_{HEX}	**7:0**	FW_Minor_Rev_L	R	0x30	Minor firmware revision low byte
0007_{HEX}	**7:0**	FW_Minor_Rev_H	R	0x05	Minor firmware revision high byte

Table 8. Read Register – Status Registers

REG	Bit	Field	Type	Default	Description
0034_{HEX}	**7**	Vout_Status	R	0_{BIN}	“0” output voltage is off. “1” output voltage is on.
0034_{HEX}	**6**	Reserved	R	0_{BIN}	Minor firmware revision high byte
0034_{HEX}	**5**	Reserved	R	0_{BIN}	
0034_{HEX}	**4**	Reserved	R	0_{BIN}	
0034_{HEX}	**3**	Reserved	R	0_{BIN}	
0034_{HEX}	**2**	Thermal_SHTDN_Status	R	0_{BIN}	“0” indicates no over-temperature condition exists. “1” indicates that the die temperature exceeds 130°C or the NTC reading is less than 0.6V. The CWR510Q sends an End Power Transfer (EPT) packet to the transmitter.
0034_{HEX}	**1**	VRECT_OV_Status	R	0_{BIN}	“1” indicates the rectifier voltage exceeds 20V for VOUT=12V. In this case, the CWR510Q sends an End Power Transfer (EPT) packet to the transmitter.
0034_{HEX}	**0**	Current_Limit_Status	R	0_{BIN}	“1” indicates the current limit has been exceeded. In this case, the CWR510Q sends an End Power Transfer (EPT) packet to the transmitter.
0035_{HEX}	**7:0**	Reserved	R	00_{HEX}	

Table 9. Read Register – Interrupt Status Registers

REG	Bit	Field	Type	Default	Description
0036_{HEX}	**7**	INT_Vout_Status	R	0_{BIN}	“0” indicates the output voltage has not changed. “1” indicates the output voltage changed.
0036_{HEX}	**6**	Reserved	R	0_{BIN}	Minor firmware revision high byte
0036_{HEX}	**5**	Reserved	R	0_{BIN}	
0036_{HEX}	**4**	Reserved	R	0_{BIN}	
0036_{HEX}	**3**	Reserved	R	0_{BIN}	
0036_{HEX}	**2**	INT_OVER_TEMP_Status	R	0_{BIN}	“1” indicates an over-temperature condition exists.
0036_{HEX}	**1**	INT_VRECT_OV_Status	R	0_{BIN}	“1” indicates a rectifier over-voltage condition exists.

0036_{HEX}	**0**	INT_OC_Limit_Status	R	0_{BIN}	"1" indicates the current limit has been exceeded.
0037_{HEX}	**7:0**	Reserved	R	00_{HEX}	

Note: If any bit in the Interrupt Status register 36HEX is "1" and the corresponding bit in the Interrupt Enable regist er 38HEX is set to "1," the INT pin will be pulled down indicating an interrupt event has occurred.

Table 10. Read Register – Interrupt Enable Registers

REG	Bit	Field	Type	Default	Description
0038_{HEX}	**7**	Vout_Status_INT_EN	R/W	0_{BIN}	"0" disables the INT_Vout_Status interrupt. "1" enables the interrupt.
0038_{HEX}	**6**	Reserved	R	0_{BIN}	
0038_{HEX}	**5**	Reserved	R	0_{BIN}	
0038_{HEX}	**4**	Reserved	R	0_{BIN}	
0038_{HEX}	**3**	Reserved	R	0_{BIN}	
0038_{HEX}	**2**	OVER_TEMP_INT_EN	R	1_{BIN}	"0" disables the INT_OVER_TEMP interrupt. "1" enables the interrupt.
0038_{HEX}	**1**	VRECT_OV_INT_EN	R/W	1_{BIN}	"0" disables the INT_VRECT_OV interrupt. "1" enables the interrupt.
0038_{HEX}	**0**	OC_Limit_Status_INT_EN	R/W	1_{BIN}	"0" disables the INT_OC_Limit_Status interrupt. "1" enables the interrupt.
0039_{HEX}	**7:0**	Reserved	R/W	00_{HEX}	

Table 11. Read Register – Battery Charge Status

REG	Bit	Field	Type	Default	Description
$003A_{HEX}$	**7:0**	Batt_Charg_status	R/W	FF_{HEX}	Battery charge status value sent to transmitter.[a]

[a] Firmware only forwards the data from the application processor to transmitter.

Table 12. Read Register – End Power Transfer

REG	Bit	Field	Type	Default	Description
$003B_{HEX}$	**7:0**	EPT_Code	R/W	FF_{HEX}	EPT_Code sent to transmitter.

Table 13. Read Register – Output Voltage of the Rectifier (VRECT)

$V_{RECT} = VRECT[15:0] \times 1[mV]$

REG	Bit	Field	Type	Default	Description
0040_{HEX}	**7:0**	VRECT[7:0]	R	-	8 LSB of VRECT voltage in mV
0041_{HEX}	**7:0**	VRECT[15:8]	R	-	8 MSB of VRECT voltage in mV

Table 14. Read Register – Output Voltage of the Main LDO (VOUT)

$V_{OUT} = VOUT \times 1[mV]$

REG	Bit	Field	Type	Default	Description
$003C_{HEX}$	**7:0**	VOUT[7:0]	R	-	8 LSB of VOUT voltage in mV
$003D_{HEX}$	**7:0**	VOUT[15:8]	R	-	8 MSB of VOUT voltage in mV

Table 15. Read Register – Output Current of the ISEN (IOUT)

$I_{OUT} = IOUT[15:0] \times 1[mA]$

REG	Bit	Field	Type	Default	Description
0044_{HEX}	**7:0**	IOUT[7:0]	R	-	8 LSB of IOUT current in mA
0045_{HEX}	**7:0**	IOUT[15:8]	R	-	8 MSB of IOUT current in mA

Table 16. Read Register – DIE Temperature

Fop = DIE_TEMP[15:0] ÷ 10[°C]

REG	Bit	Field	Type	Default	Description
0046_{HEX}	**7:0**	DIE_Temp[7:0]	R	-	8 LSB of current die temperature in °C.
0047_{HEX}	**7:0**	DIE_Temp[15:8]	R	-	8 MSB of current die temperature in °C.

Table 17. Read Register – Operating Frequency

Fop = OP_FREQ[15:0] ÷ 10[kHz]

REG	Bit	Field	Type	Default	Description
0048_{HEX}	**7:0**	OP_FREQ[7:0]	R	-	8 LSB of the AC signal frequency in kHz.
0049_{HEX}	**7:0**	OP_FREQ[15:8]	R	-	8 MSB of the AC signal frequency in kHz.

Table 18. Read Register – ALIGNX

REG	Bit	Field	Type	Default	Description
$004B_{HEX}$	**7:0**	Align_X	R	-	8-bit signed integer representing alignment between Tx and Rx coil in the X-direction. The value is application-specific.

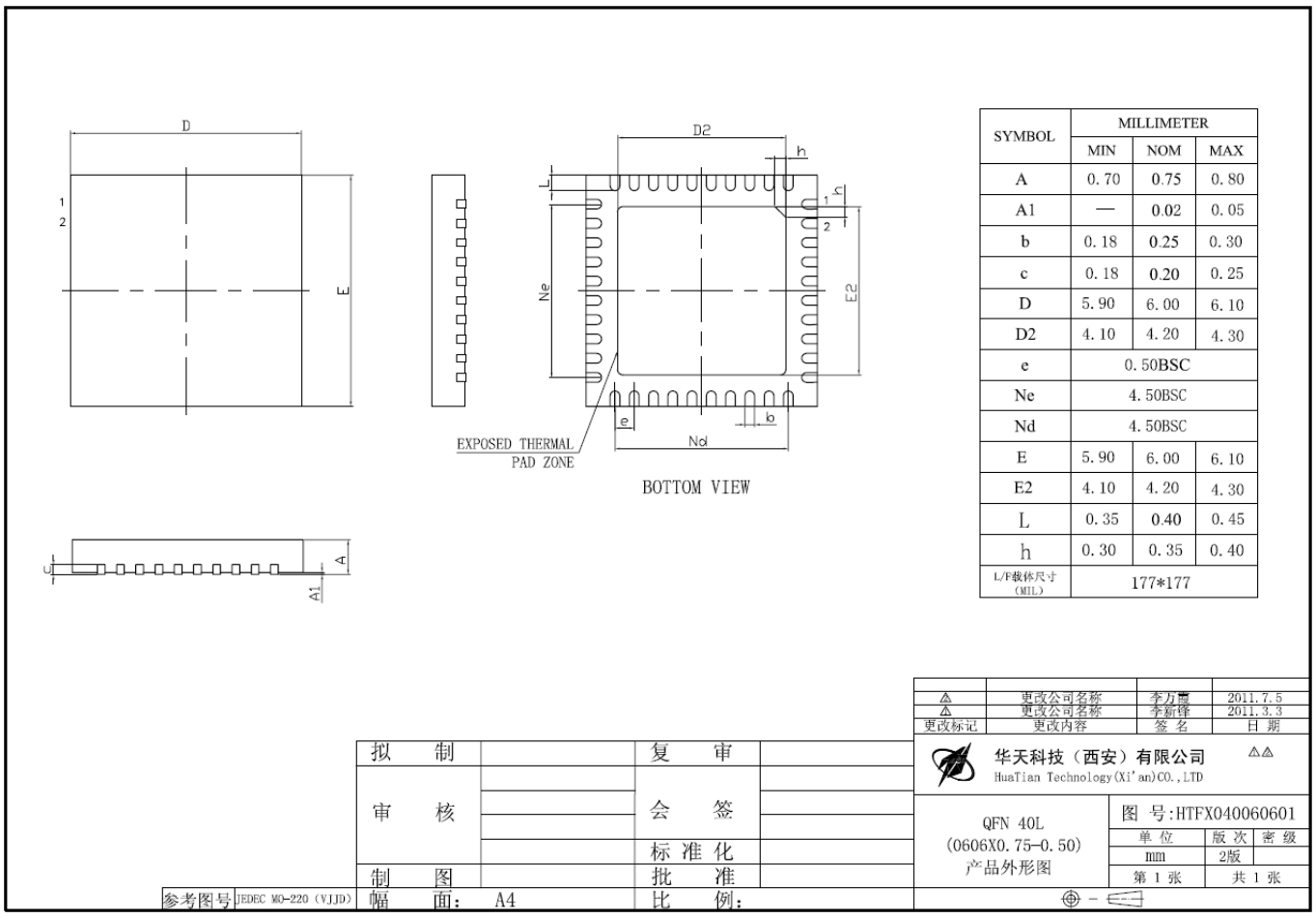
Table 19. Read Register – ALIGNY

REG	Bit	Field	Type	Default	Description
$004C_{HEX}$	**7:0**	Align_Y	R	-	8-bit signed integer representing alignment between Tx and Rx coil in the Y-direction. The value is application-specific.

Table 20. Read Register – Command Register

REG	Bit	Field	Type	Default	Description
$004E_{HEX}$	**7:6**	Reserved	R	0_{HEX}	Reserved.
$004E_{HEX}$	**5**	Clear_Interrupt	R/W	0_{HEX}	If application processor sets this bit to "1," the CWR510Q clears the interrupt pin.
$004E_{HEX}$	**4**	Send_Battery_Charge_Status packet	R	0_{HEX}	If the application processor sets this bit to "1," the CWR510Q sends the charge status packet once (from the Batt_Charge_status register; see Table 15) and then sets this bit to "0."
$004E_{HEX}$	**3**	Send_End_Power_Transfer	R/W	0_{HEX}	If application processor sets this bit to "1," the CWR510Q sends the end power transfer packet (defined in the EPT_Code register in Table 16) to the transmitter and then sets this bit to "0."
$004E_{HEX}$	**2**	Reserved	R	0_{HEX}	Reserved
$004E_{HEX}$	**1**	Toggle_LDO_On-OFF	R/W	0_{HEX}	If application processor sets this bit to "1," the CWR510Q toggles the LDO output once (from on to off or from off to on), and then sets this bit to "0."
0038_{HEX}	**0**	Reserved	R	0_{HEX}	Reserved

4. Package Outline



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	5.90	6.00	6.10
D2	4.10	4.20	4.30
e	0.50BSC		
Ne	4.50BSC		
Nd	4.50BSC		
E	5.90	6.00	6.10
E2	4.10	4.20	4.30
L	0.35	0.40	0.45
h	0.30	0.35	0.40
L/F载体尺寸 (MIL)	177*177		

更改标记	更改内容	签 名	日 期
△	更改公司名称	李万雷	2011.7.5
△	更改公司名称	李新锋	2011.3.3

拟 制		复 审	
审 核		会 签	
		标准化	
制 图		批 准	
参考图号 JEDEC MO-220 (VJJD)	幅 面: A4	比 例:	

华天科技（西安）有限公司
HuaTian Technology(Xi'an)CO.,LTD

QFN 40L
(0606X0.75-0.50)
产品外形图

图 号:HTFX040060601

单 位	版 次	密 级
mm	2版	
第 1 张	共 1 张	

Figure 4. QFN 40pin Package Outline, 6.00mm x 6.00mm, 0.5mm pitch

5. Electrical Characteristics

5.1 Absolute Maximum Rating

PIN	Parameter	Rating	Unit
AC1, AC2, COMM1, COMM2, VRECT, SINK, RSV4_CMA, RSV5_CMB	Voltage	-0.3 to 20	V
BOOST1, BOOST2	Voltage	-0.3 to 26	V
VOUT, RSV2, RSV3	Voltage	-0.3 to 15	V
LDO50, ENB, SDA, SCL, ALIGNY, ALIGNX, INTB, RSV1_ANATEST	Voltage	-0.3 to 6	V
LDO18, TS_EOC, VOSET_QF, RPPG, RPPO, ILIM, DEN_DIGTEST,	Voltage	-0.3 to 2	V
PGND, AVSS	Voltage	-0.3 to 0.3	V
AC1, AC2, VRECT, VOUT, PGND	RMS Current	2	A
SINK	Current	1	A
COMM1, COMM2, RSV4_CMA, RSV5_CMB	RMS Current	500	mA

5.2 Recommended Operating Condition

Symbol	Description	Min.	Typ.	Max.	Unit
V_{RECT}	Rectifier voltage range	4		10	V
I_{OUT}	Main LDO output current			1.7	A
I_{COMM}	COMM1, COMM2 sink current			500	mA
T_J	Junction temperature	-30		125	℃
T_A	Ambient temperature	-30		85	℃

5.3 Thermal Information

Parameters	CWR510Q QFN 40pin 6.00mm x 6.00mm	UNITS
Junction-to-ambient thermal resistance		℃/W
Junction-to-case thermal resistance		℃/W
Junction-to-board thermal resistance		℃/W
Junction temperature，T_J		℃
Ambient operation temperature		℃
Storage temperature，T_{stg}		℃
Lead soldering temperature，T_L(10s)		℃

5.4 ESD

Test Model	RATINGS	UNITS
HBM: all pins	2000	V
CDM: all pins	500	V

5.5 ELECTRICAL Characteristics

Unless otherwise specified: T_A = -20°C to 70°C. Typical values are for T_A = 25°C

Symbol	Description	Conditions	Min.	Typ.	Max.	Unit
Synchronous Active Rectifier						
V_{IN_RECT}	AC1, AC2 input voltage range		4.0		15	V
f_{IN_RECT}	AC1, AC2 input frequency range		80		500	kHz
E_{ff_RECT}	AC to DC power conversion efficiency			92		%
V_{UVLO}	Under voltage lockout	V_{RECT}: 0V to 4V		3.1	3.2	V
V_{UVLO_HYS}	Under voltage lockout hysteresis	V_{RECT}: 4V to 0V		150		mV
Main LDO						
V_{IN_MLDO}	Main LDO input voltage range		4.0		10	V
V_{OUT}	Main LDO output voltage range Register programmable	V_{RECT}>5V	3.5		7	V
$V_{OUT\_MLDO\_STEP}$	Main LDO output voltage control step			25		mV
I_{OUT_MLDO}	Main LDO output current range	V_{OUT}≤7V			1.7	A
P_{SRR_MLDO}	Main LDO power supply rejection ratio	C_{VOUT}=20uF DC to 100MHz	20			dB
Internal LDO						
V_{LDO50}	Internal LDO50 output voltage	V_{RECT}>5V, C_{LDO50}=1uF, External load<30mA	4.62	5	5.38	V
V_{LDO18}	Internal LDO18 output voltage	V_{RECT}>3V, C_{LDO18}=1uF External load<30mA		1.8		V
BGR						
V_{BGR}	Internal BGR output voltage Register programmable	V_{RECT}>3V		1.22		V
Oscillator						
f_{OSC}	Internal oscillator frequency Register programmable	V_{RECT}>3V		15		MHz
ADC						
N_{ADC}	ADC resolution	V_{RECT}>3V		12		bit
f_{SAMPLE}	ADC sampling rate	f_{OSC}=15MHz		217		kSa/s
N_{CH_ADC}	ADC channel			7		
ENB/CHG_DOWN						
V_{IH}	ENB/CHG_DOWN input threshold high		1.5			V

V_{IL}	ENB/CHG_DOWN input threshold low				0.5	V
Protection						
V_{OVP_H}	VRECT over voltage protection detection level Register programmable	V_{RECT}: 5V to 16V	14	15	21	V
V_{OVP_L}	VRECT over voltage protection release level Register programmable	V_{RECT}: 16V to 5V	12	14	19	V
I_{OCL}	I_{OUT} over current limit protection Programmable by R_{IL1} and R_{IL2}	R_{IL1}= 10kΩ R_{IL2}= 5kΩ I_{OUT}: 0A to 2A		1.6	2.0	A
T_{OTP}	Over temperature protection Thermal shutdown temperature	Temperature: 30℃ to 160℃		150		℃
T_{OTP_HYS}	OTP hysteresis	Temperature: 160℃ to 30℃		20		℃
VOSET_QF, ILIM, TS_EOC, RPPO, RPPG, DEN_DIGTEST (Note1)						
I_{GPIO_LKG}	Input Leakage Current	V_{OSET_QF},V_{LIM} ,V_{TS_EOC} ,V_{RPPO} , V_{RPPG}, $V_{DEN\_DIGTEST}$=0V and 1.8V	-1		1	uA
ALIGN X (Note1)						
I_{ALIGH_LKG}	Input Leakage Current	V_{ALIGNX} = 0V and 5V	-1		1	uA
I2C Interface – SCL, SDA and INTB						
I_{LKG_LOW}	Input Current @ENB = LOW	V_{SCA}, V_{SDA}, V_{INTB} = 0V and 5V	-1		1	uA
I_{LKG_HIGH}	Input Current @ENB = HIGH	V_{SCA}, V_{SDA}, V_{INTB} = 0V and 5V	-1		1	uA
VRECT and VOUT						
I_{RECT}	Input Leakage Current	V_{RECT} = 5V		2.8		uA
		V_{RECT} = 9V		5.9		uA
		V_{RECT} = 12V		9.0		uA
I_{OUT}	Input Leakage Current	V_{OUT} = 5V		13.8		uA
		V_{OUT} = 9V		28.1		uA
		V_{OUT} = 12V		39.9		uA

Note1) Condition : VRECT =5.0V, C_{VOUT}=10uF, ENB = LOW

6. I²C Signal Timing

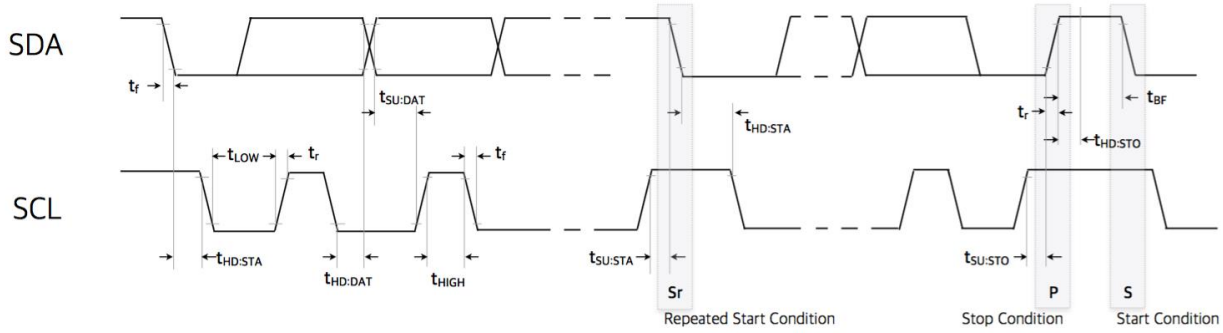


Figure 7. Timing Diagram for I²C interface

Table 3. I²C Characteristics

Symbol	Description	Conditions	Min.	Typ.	Max.	Unit
V_{IL_SDA}	Input low threshold level SDA	V_{PULLUP}=LDO18=1.8V			0.6	V
V_{IH_SDA}	Input high threshold level SDA	V_{PULLUP}=LDO18=1.8V	1.5			V
V_{IL_SCL}	Input low threshold level SCL	V_{PULLUP}=LDO18=1.8V			0.6	V
V_{IH_SCL}	Input high threshold level SCL	V_{PULLUP}=LDO18=1.8V	1.5			V
f_{SCL}	SCL clock frequency				400	kHz
t_{LOW}	SCL clock low time		1.3			us
t_{HIGH}	SCL clock high time		0.6			us
t_r	Rise time of both SDA and SCL				0.3	us
t_f	Fall time of both SDA and SCL				0.3	us
$t_{SU,STA}$	Setup time for START condition		0.6			us
$t_{HD,STA}$	Hold time for START condition		0.6			us
$t_{SU,DAT}$	Data setup time		0.1			us
$t_{HD,DAT}$	Data hold time				0.9	us
$t_{SU,STO}$	Setup time for STOP condition		0.6			us
t_{BF}	Bus free time between STOP and START condition		1.3			us

7. Typical Application Schematic and BOM

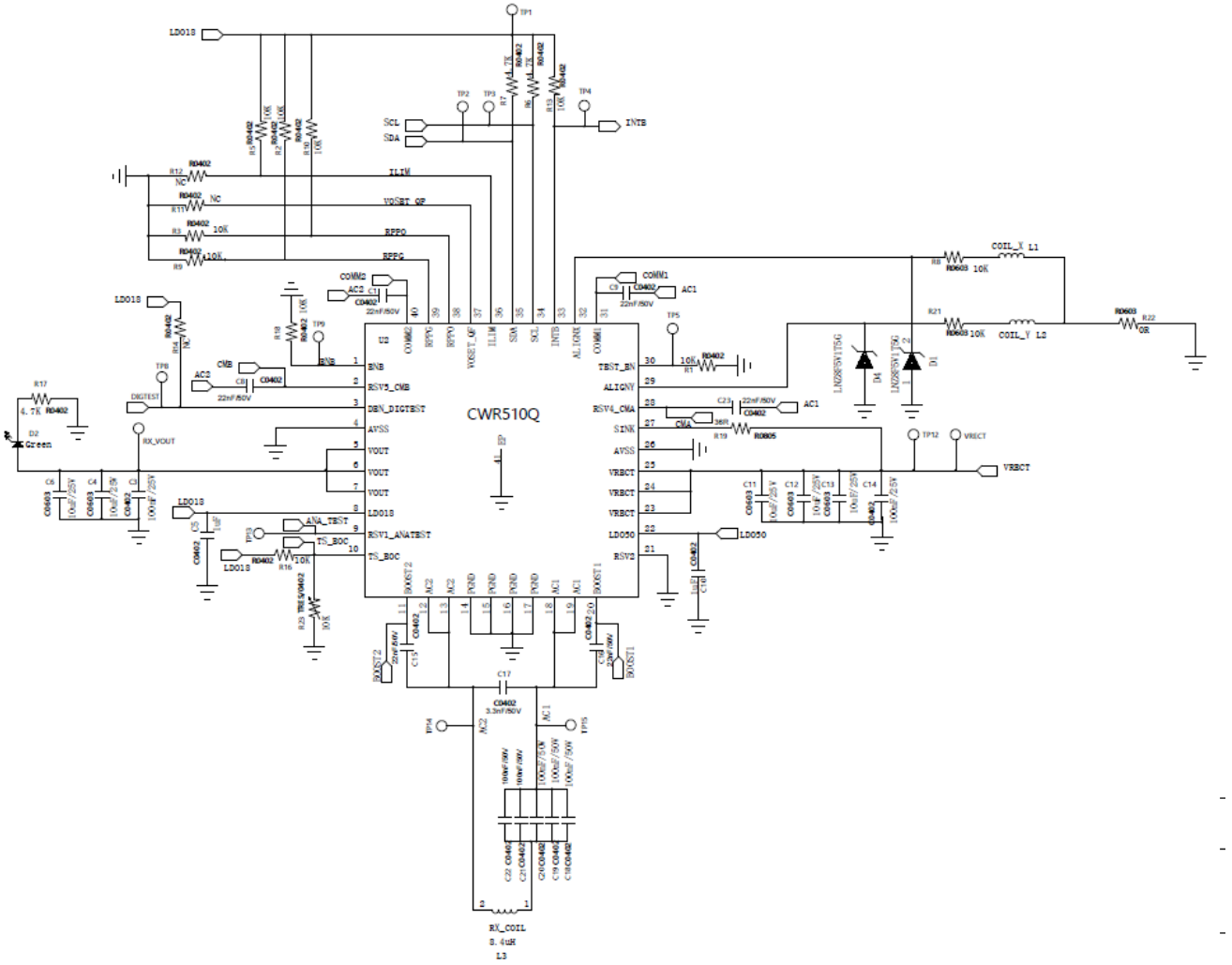


Figure 8. CWR510Q Typical Application schematic

Table 4. CWR510Q Evaluation Board V1.0 BOM

ITEM	REF-DES	QTY	Value	Description	Manufacturer	PCB DECAL
1	L1	1		AlignX Coil		RX_COIL/3X4
2	L2	1		AlignY Coil		RX_COIL/3X4
3	U2	1	CWR510Q	Qi Compliant Wireless Power Receiver IC	Celfras Semiconductor Inc	QFN40
5	L3	1	8.4uH	WIRELESS CHARGING COIL ASSEMBLY	Sunlord	RX_COIL/3X4
6	C3 C14	2	100nF/25V	CAP CER 0.1UF 25V X7R 0402 ±10%	Murata Electronics North America	C0402
7	C18-22	5	100nF/50V	CAP CER 0.1UF 50V X7R 0402 ±10%	Murata Electronics North America	C0402
8	C5 C10	2	1uF	CAP CER 1UF 25V X5R 0402 ±10%	Murata Electronics North America	C0402
9	C1 C8-9 C15-16 C23	6	22nF/50V	CAP CER 0.022UF 50V X7R 0402 ±10%	Murata Electronics North America	C0402
10	C17	1	3.3nF/50V	CAP CER 3300PF 50V X7R 0402 ±5%	Murata Electronics North America	C0402
11	C4 C6 C11-13	5	10uF/25V	CAP CER 10UF 25V X5R 0603 ±20%	Murata Electronics North America	C0603
12	R22	1	0R	RES SMD 0 OHM 1% 1/16W 0402	Yageo	R0603
13	R1-3 R5 R9-10 R13 R16 R18	9	10K	RES SMD 10K OHM 1% 1/16W 0402	Yageo	R0402
14	R8 R21	2	10K	RES SMD 10K OHM 1% 1/16W 0402	Yageo	R0603
15	R6-7	2	4.7K	RES SMD 4.7K OHM 1% 1/16W 0402	Yageo	R0402
17	R19	1	36R	RES SMD 36 OHM 1% 1/8W 0805	Yageo	R0805
20	R23	1	10K	NTC THERMISTOR 10K OHM 1% 0402	TDK Corporation	TRES/0402
21	D1 D4	2	LNZ8F5V1T5G	GENERIC ZENER-DIODE	LRC	0201/5
		43				
16	R11-12 R14	3	NC	RES SMD 10K OHM 1% 1/16W 0402	Yageo	R0402
18	RX_VOUT VRECT	2				TP/SMD/5015/1.78X3.43
19	TP2-5 TP8-9 TP12-15 TP1	11				TP/SMD/D1.0
4	D2	1	Green	LED,GREEN,0603	HQ	LED/0603
	R17	1	4.7K	RES SMD 4.7K OHM 1% 1/16W 0402	Yageo	R0402

Revision History

Date	Version No.	Description
2019/12/10	1.0	Preliminary Release
2020/01/09	1.1	Updated VOUT/IOUT equation and parameter corresponding to our algorithm and updated the latest schematic and BOM
2020/02/12	1.2	Modified OCL related equations and updated VRECT/VOUT/Current/OP_FREQ equation. Corrected to some typos。

Ordering Information

Part Number	Package Type	Shipping Carrier	Package Qty	Eco Plan	MSL Peak Temp	Description	Device Marking
CWR510Q	QFN 40pin, 6.0mm x 6.0mm	Tape and Reel		Green (RoHS&noSb/Br)	Level-3-260C-UNLIM		