

• General Description

The AGM412MAP combines advanced trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$. This device is ideal for load switch and battery protection applications.

• Features

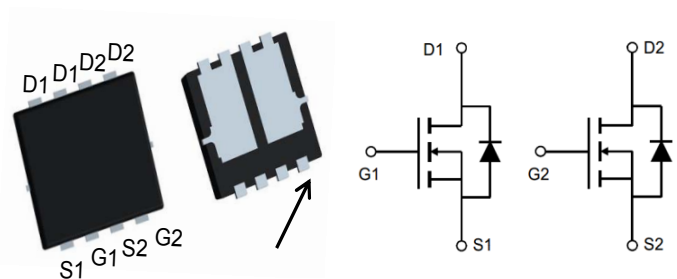
- Advance high cell density Trench technology
- Low $R_{DS(ON)}$ to minimize conductive loss
- Low Gate Charge for fast switching
- Low Thermal resistance

• Application

- MB/VGA Vcore
- SMPS 2nd Synchronous Rectifier
- POL application
- BLDC Motor driver

Product Summary

BVDSS	RDSON	ID
40V	12mΩ	22A

PDFN3.3X3.3 Pin Configuration

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
AGM412MAP	AGM412MAP	DFN3.3*3.3	325mm	16mm	5000

Maximum ratings, at $T_j=25\text{ }^\circ\text{C}$, unless otherwise specified

Symbol	Parameter	Rating	Unit
$V_{(BR)DSS}$	Drain-Source breakdown voltage	40	V
I_S	Diode continuous forward current	$T_C = 25^\circ\text{C}$ 22	A
I_D	Continuous drain current @ $V_{GS}=10\text{V}$	$T_C = 25^\circ\text{C}$ 20	A
		$T_A = 100^\circ\text{C}$ 15	A
I_{DM}	Pulse drain current tested ①	$T_C = 25^\circ\text{C}$ 80	A
EAS	Avalanche energy, single pulsed ②	$I_D=10\text{A}$ 15	mJ
P_D	Maximum power dissipation	$T_A = 25^\circ\text{C}$ 35	W
V_{GS}	Gate-Source voltage	± 20	V
T_{STG} T_J	Storage and operating temperature range	-55 to 150	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	Typical	Unit
$R_{\theta JC}$	Thermal Resistance-Junction to Case	3.5	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient	50	$^\circ\text{C/W}$

Typical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ T_c = 25°C (unless otherwise stated)						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V I _D =250μA	40	--	--	V
I _{DSS}	Zero Gate Voltage Drain Current(T _c =25°C)	V _{DS} =40V, V _{GS} =0V	--	--	1	μA
	Zero Gate Voltage Drain Current(T _c =125°C)	V _{DS} =40V, V _{GS} =0V	--	--	100	μA
I _{GSS}	Gate-Body Leakage Current	V _{GS} =±20V, V _{DS} =0V	--	--	±100	nA
V _{GS(TH)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	1.0	1.7	2.5	V
R _{DS(ON)}	Drain-Source On-State Resistance ^③	V _{GS} =10V, I _D =15A	--	12	18	mΩ
R _{DS(ON)}	Drain-Source On-State Resistance ^③	V _{GS} =4.5V, I _D =10A	--	18	25	mΩ
R _{DS(ON)}	Drain-Source On-State Resistance ^③	V _{GS} =4.2V, I _D =2A	--	20	28	mΩ
Dynamic Electrical Characteristics @ T_c = 25°C (unless otherwise stated)						
C _{iss}	Input Capacitance	V _{DS} =15V, V _{GS} =0V, f=1MHz	--	475	--	pF
C _{oss}	Output Capacitance		--	75	--	pF
C _{rss}	Reverse Transfer Capacitance		--	45	--	pF
Q _g	Total Gate Charge	V _{DS} =15V, I _D =10A, V _{GS} =10V	--	13	--	nC
Q _{gs}	Gate-Source Charge		--	3.5	--	nC
Q _{gd}	Gate-Drain Charge		--	2.5	--	nC
Switching Characteristics						
t _{d(on)}	Turn-on Delay Time	V _{DD} =15V, I _D =10A, R _G =6.8Ω, V _{GS} =10V	--	6	--	nS
t _r	Turn-on Rise Time		--	12	--	nS
t _{d(off)}	Turn-Off Delay Time		--	18	--	nS
t _f	Turn-Off Fall Time		--	7	--	nS
Source- Drain Diode Characteristics @ T_c = 25°C (unless otherwise stated)						
V _{SD}	Forward on voltage	I _{SD} =15A, V _{GS} =0V	--	0.86	1.2	V
t _{rr}	Reverse Recovery Time	T _j =25°C, I _{sd} =10A, V _{GS} =0V di/dt=100A/μs	--	19	--	nS
Q _{rr}	Reverse Recovery Charge		--	26	--	nC

NOTE:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Limited by T_{Jmax}, starting T_J = 25°C, L = 0.3mH, R_G = 25Ω, I_{AS} = 10A, V_{GS} = 10V. Part not recommended for use above this value
- ③ Pulse width ≤ 300μs; duty cycle ≤ 2%.

Typical Characteristics

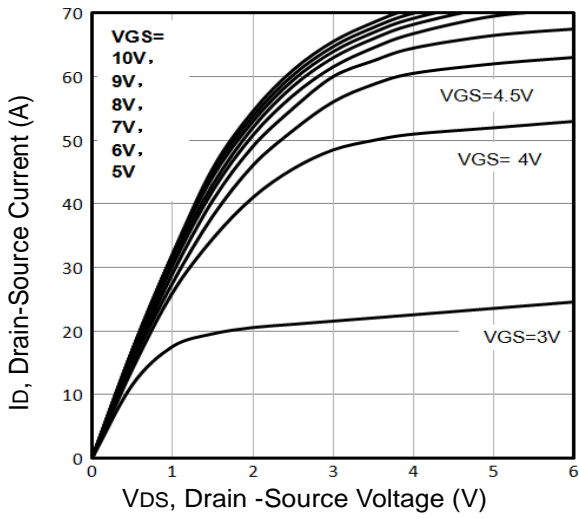


Fig1. Typical Output Characteristics

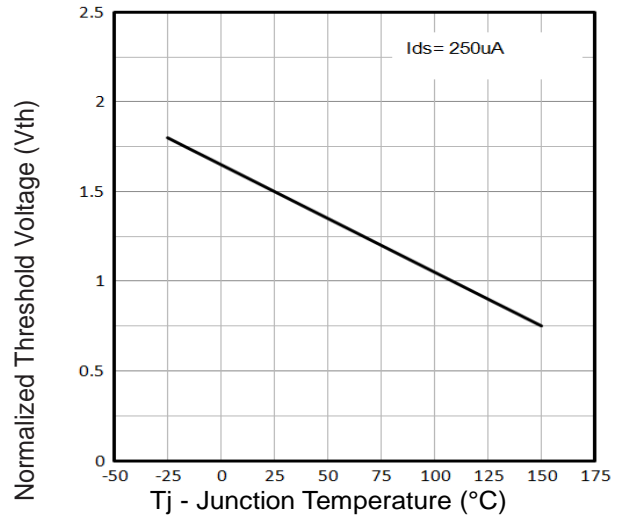


Fig2. Normalized Threshold Voltage Vs. Temperature

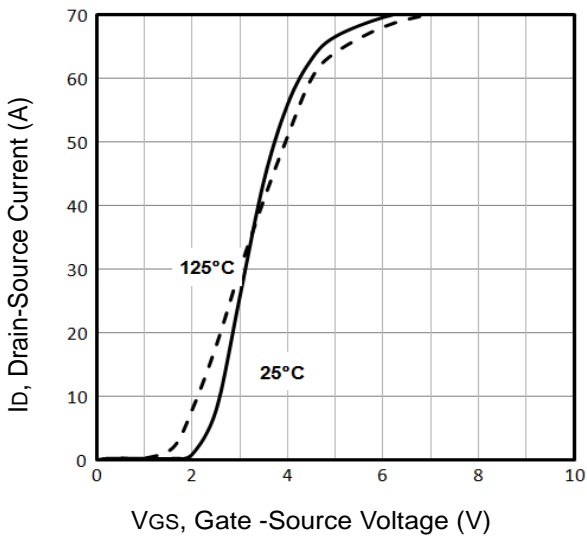


Fig3. Typical Transfer Characteristics

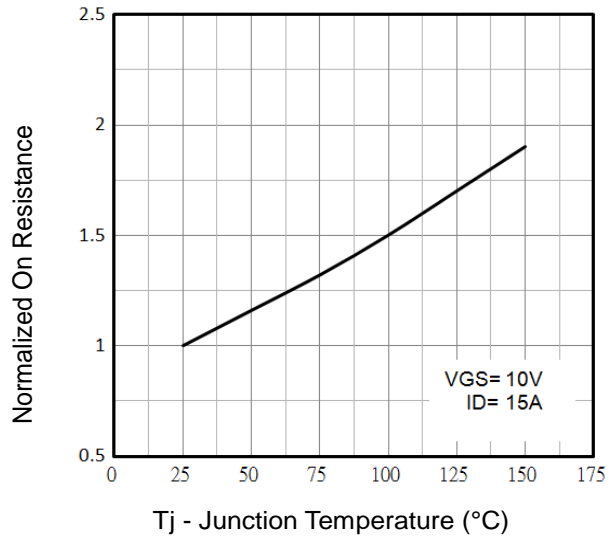


Fig4. Normalized On-Resistance Vs. Temperature

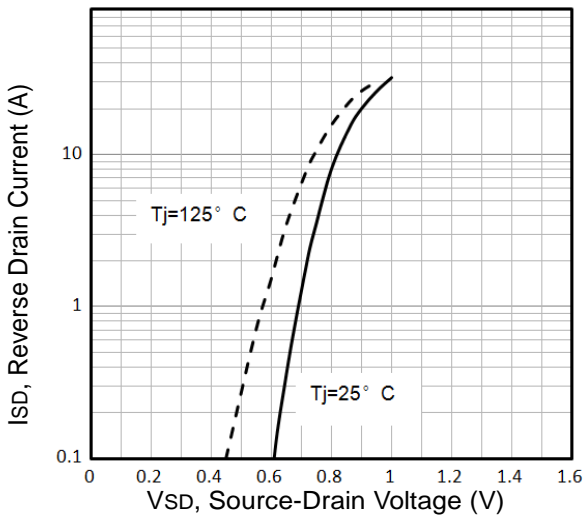


Fig5. Typical Source-Drain Diode Forward Voltage

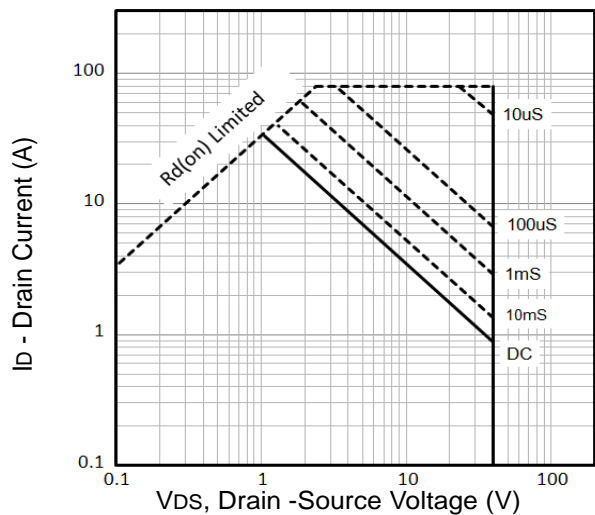


Fig6. Maximum Safe Operating Area

Typical Characteristics

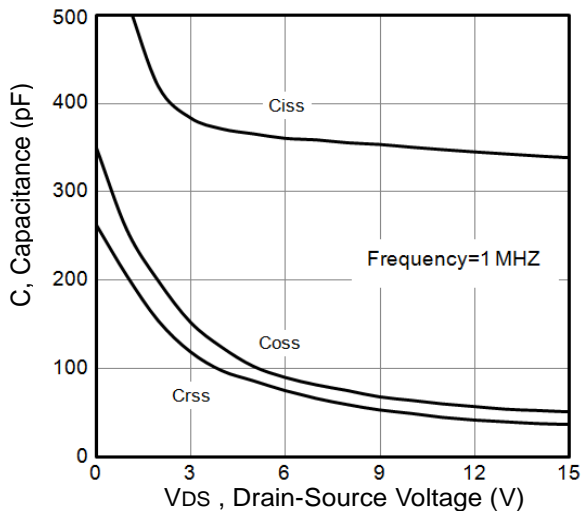


Fig7. Typical Capacitance Vs.Drain-Source Voltage

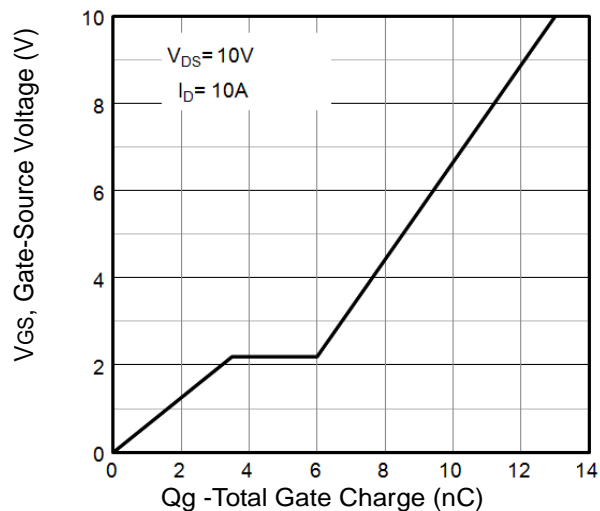


Fig8. Typical Gate Charge Vs.Gate-Source

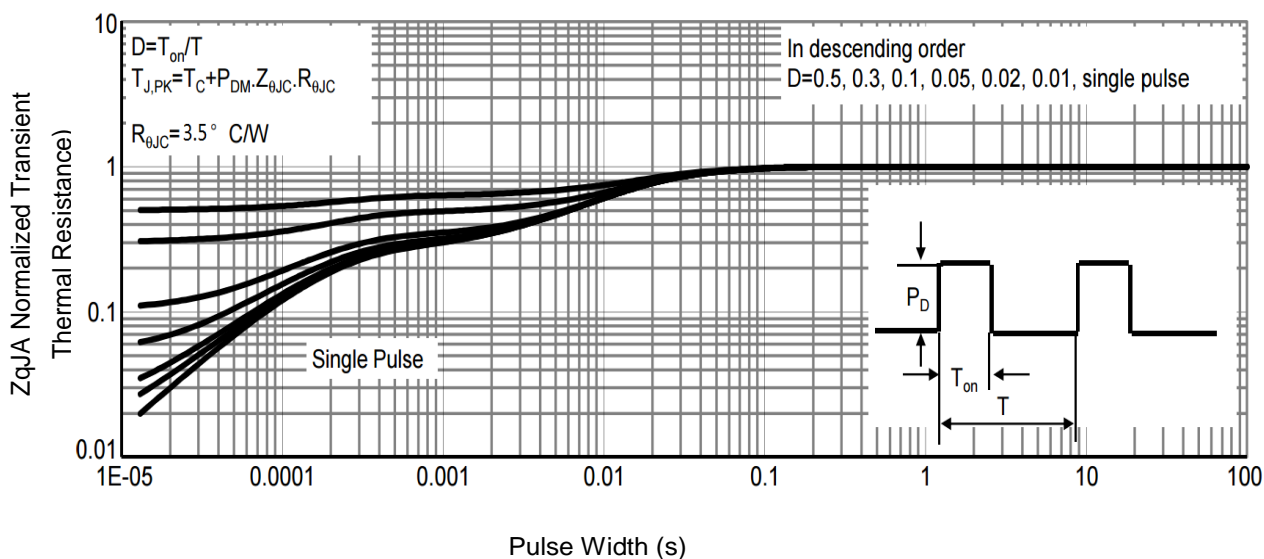


Fig 9 . Normalized Maximum Transient Thermal Impedance

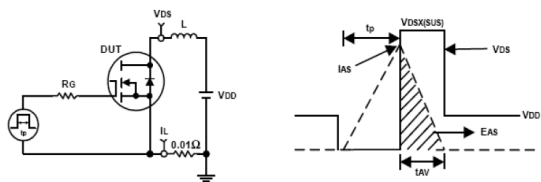


Fig10. Unclamped Inductive Test Circuit and waveforms

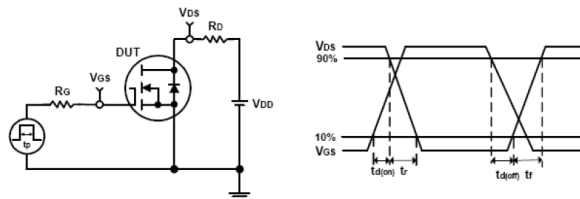
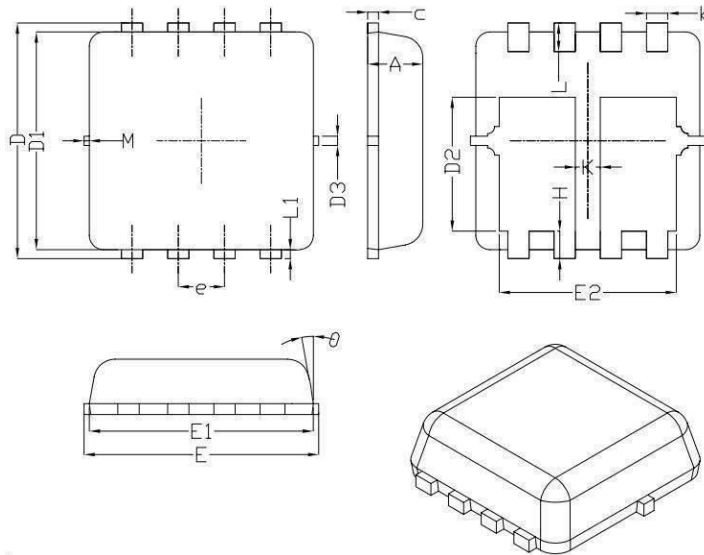


Fig11. Switching Time Test Circuit and waveforms

•Dimensions (DFN3.3×3.3)


Symbol	Dimensions (unit: mm)		
	Min	Typ	Max
A	0.70	0.75	0.80
b	0.25	0.30	0.35
c	0.10	0.15	0.25
D	3.25	3.35	3.45
D1	3.00	3.10	3.20
D2	1.78	1.88	1.98
D3	--	0.13	--
E	3.20	3.30	3.40
E1	3.00	3.15	3.20
E2	2.39	2.49	2.59
e	0.65 BSC		
H	0.30	0.39	0.50
L	0.30	0.40	0.50
L1	--	0.13	--
K	0.30	--	--
θ	--	10°	12°
M	*	*	0.15

* Not Specified


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