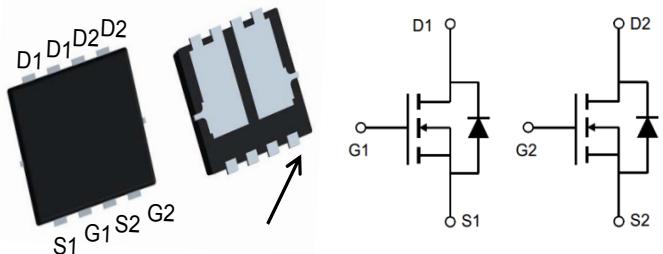


- ★ 100% EAS Guaranteed
- ★ Green Device Available
- ★ Super Low Gate Charge
- ★ Excellent CdV/dt effect decline
- ★ Advanced high cell density Trench technology

Product Summary

BVDSS	RDS(ON)	ID
30V	10.5mΩ	25A

PDFN3.3X3.3 Pin Configuration



Description

AGM311MAP is the high cell density trenched N-ch MOSFETs, which provide excellent RDS(ON) and gate charge for most of the synchronous buck converter applications.

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
AGM311MAP	AGM311MAP	DFN3.3*3.3	325mm	16mm	5000

Table 1. Absolute Maximum Ratings ($T_A=25^\circ\text{C}$)

Symbol	Parameter	Value	Unit
V_{DS}	Drain-Source Voltage ($V_{GS}=0\text{V}$)	30	V
V_{GS}	Gate-Source Voltage ($V_{DS}=0\text{V}$)	± 20	V
I_D	Drain Current-Continuous($T_c=25^\circ\text{C}$) <small>(Note 1)</small>	25	A
	Drain Current-Continuous($T_c=100^\circ\text{C}$)	20	A
IDM (pulse)	Drain Current-Continuous@ Current-Pulsed (Note 2)	40	A
P_D	Total Power Dissipation ($T_c=25^\circ\text{C}$)	40	W
	Total Power Dissipation ($T_a=25^\circ\text{C}$)	2.1	W
E_{AS}	Avalanche energy <small>(Note 3)</small>	75	mJ
T_J, T_{STG}	Operating Junction and Storage Temperature Range	-55 To 150	°C

Table 2. Thermal Characteristic

Symbol	Parameter	Typ	Max	Unit
$R_{\theta JA}$	Thermal Resistance Junction-ambient (Steady State) ¹	---	60	°C/W
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	---	10	°C/W

Table 3. Electrical Characteristics (TA=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
On/Off States						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V I _D =250μA	30			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =30V, V _{GS} =0V			1	μA
I _{GSS}	Gate-Body Leakage Current	V _{GS} =±20V, V _{DS} =0V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	1.2	1.6	2.5	V
g _{FS}	Forward Transconductance	V _{DS} =10V, I _D =5A		10		S
R _{DSON}	Drain-Source On-State Resistance	V _{GS} =10V, I _D =15A		10.5	15	mΩ
		V _{GS} =4.5V, I _D =15A		15	22	mΩ
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{DS} =15V, V _{GS} =0V, F=1MHZ		850		pF
C _{oss}	Output Capacitance			130		pF
C _{rss}	Reverse Transfer Capacitance			98		pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1.0MHz		1.9		Ω
Switching Times						
t _{d(on)}	Turn-on Delay Time	V _{GS} =10V, V _{DS} =15V, R _L =0.75Ω, R _{GEN} =3.3Ω		4.7		nS
t _r	Turn-on Rise Time			11		nS
t _{d(off)}	Turn-Off Delay Time			17		nS
t _f	Turn-Off Fall Time			5.6		nS
Q _g	Total Gate Charge	V _{GS} =10V, V _{DS} =15V, I _D =10A		10		nC
Q _{gs}	Gate-Source Charge			4		nC
Q _{gd}	Gate-Drain Charge			6.1		nC
Source-Drain Diode Characteristics						
I _{SD}	Source-Drain Current(Body Diode)				25	A
V _{SD}	Forward on Voltage	V _{GS} =0V, I _S =20A			1.2	V

Notes 1.The maximum current rating is package limited.

Notes 2.Repetitive Rating: Pulse width limited by maximum junction temperature

Notes 3.EAS condition: T_J=25°C, V_{DD}=15V, V_G=10V, RG=25Ω

Fig.1 Power Dissipation Derating Curve

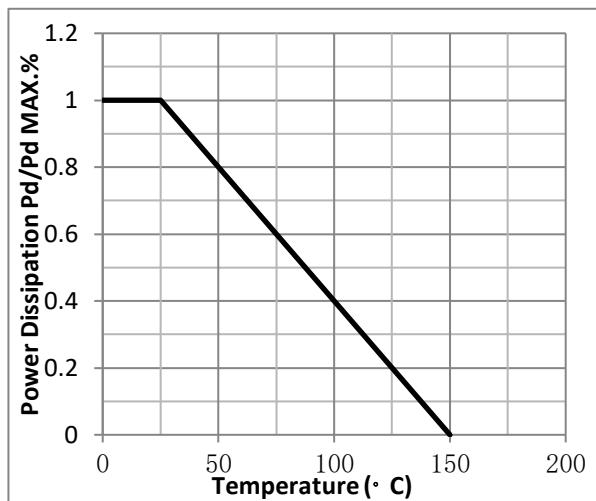


Fig.2 Typical output Characteristics

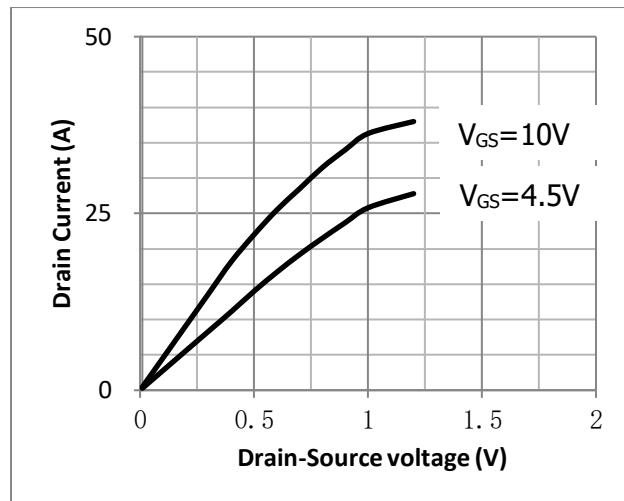


Fig.3 Threshold Voltage V.S Junction Temperature

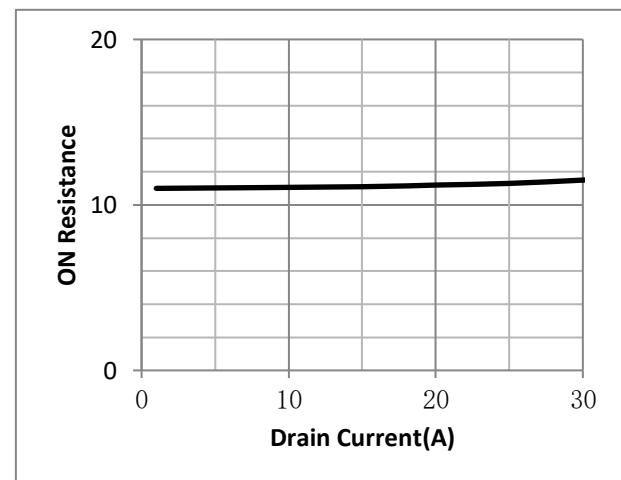
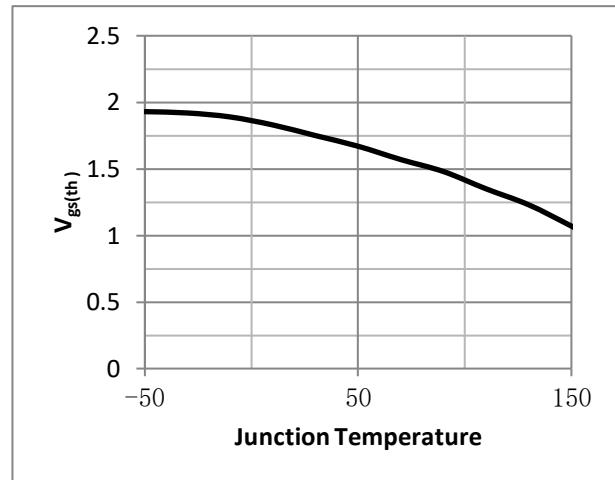


Fig.5 On-Resistance VS Gate Source Voltage

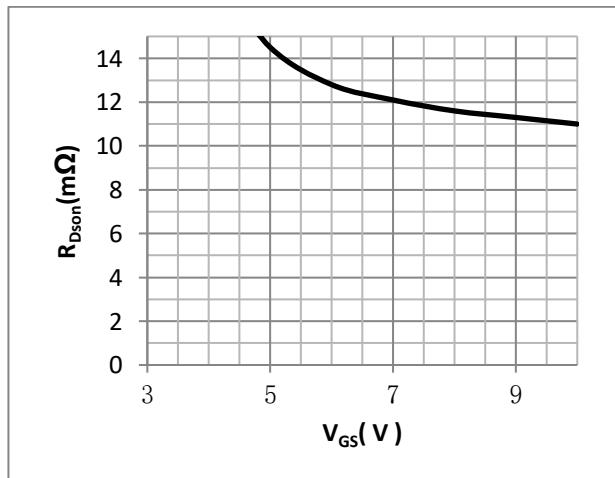


Fig.6 On-Resistance V.S Junction Temperature

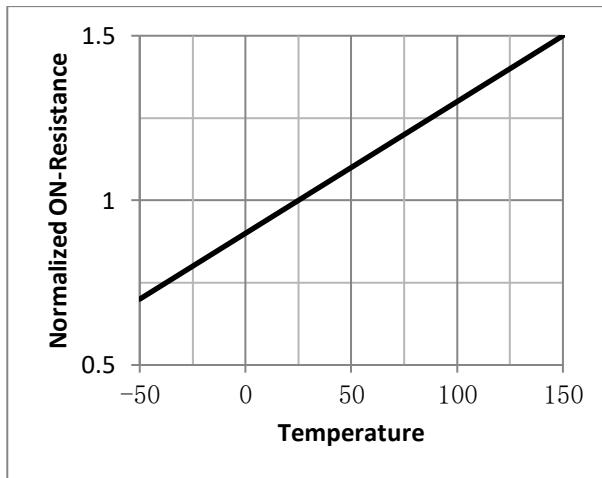


Fig.7 Switching Time Measurement Circuit

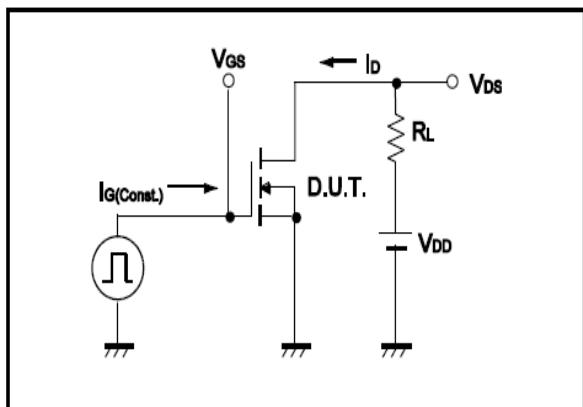


Fig.8 Gate Charge Waveform

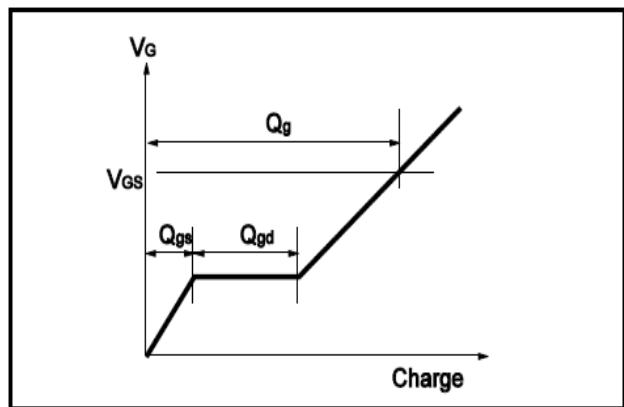


Fig.9 Switching Time Measurement Circuit

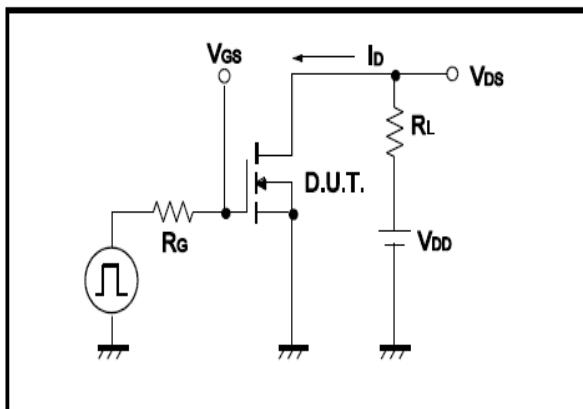


Fig.10 Gate Charge Waveform

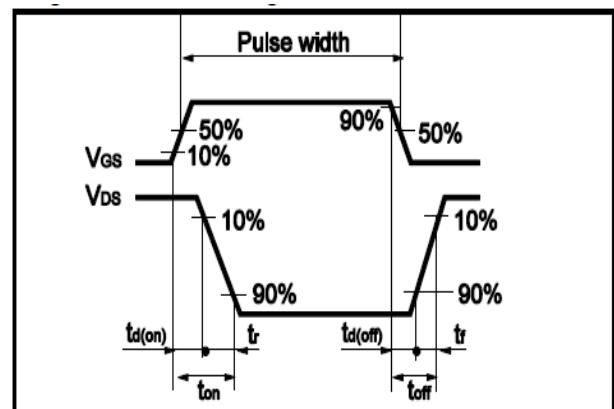


Fig.11 Avalanche Measurement Circuit

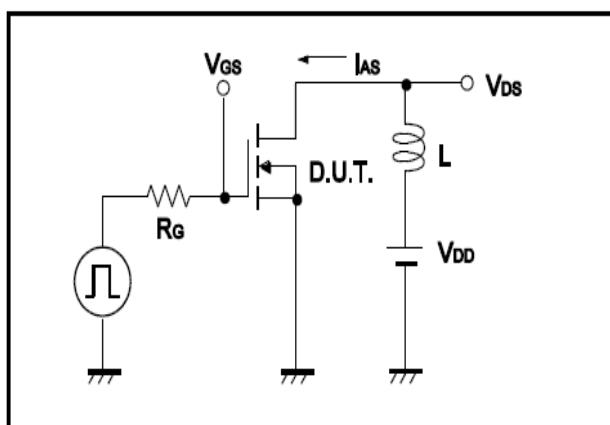
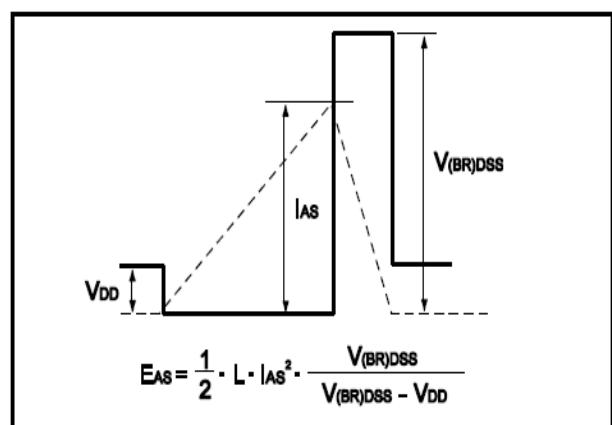
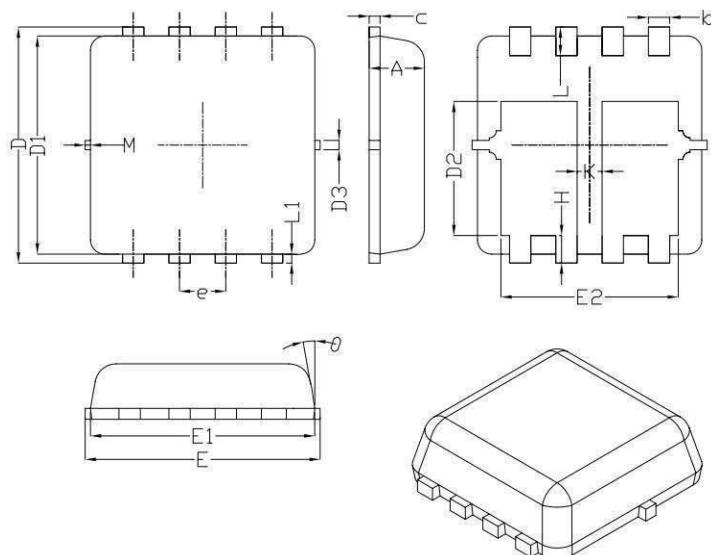


Fig.12 Avalanche Waveform



•Dimensions (DFN3.3×3.3)



Symbol	Dimensions (unit: mm)		
	Min	Typ	Max
A	0.70	0.75	0.80
b	0.25	0.30	0.35
c	0.10	0.15	0.25
D	3.25	3.35	3.45
D1	3.00	3.10	3.20
D2	1.78	1.88	1.98
D3	--	0.13	--
E	3.20	3.30	3.40
E1	3.00	3.15	3.20
E2	2.39	2.49	2.59
e	0.65 BSC		
H	0.30	0.39	0.50
L	0.30	0.40	0.50
L1	--	0.13	--
K	0.30	--	--
θ	--	10°	12°
M	*	*	0.15

* Not Specified

Disclaimer:

The information provided in this document is believed to be accurate and reliable. however, Shenzhen Core Control Electronics Technology Co., Ltd. does not assume any responsibility for the following consequencesDo not consider the use of such information or use beyond its scope.

The information mentioned in this document may be changed at any time without notice.

The products and information provided in this document do not infringe patents. Shenzhen Core Control Electronics Technology Co., Ltd. assumes no responsibility for any infringement of any other rights of third parties.The result of using such products and information.

This document is the second version issued on October 10, 2019. This document replaces andReplace all previously provided information.

 It is a registered trademark of Shenzhen Core Control Electronics Technology Co., Ltd.

Copyright © 2017 Shenzhen Core Control Electronics Technology Co., Ltd. all rights reserved.